ReadyBoard™ 800
Single Board Computer
Reference Manual

P/N 5001804A Revision D

Notice Page

NOTICE

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REVISION HISTORY

Revision	Reason for Change	Date
A, A	Initial Release	Jul/06
A, B	Updates/Changes	Oct/06
A, C	Changed location of battery	Sept/07
A, D	Changed p/n of Ethernet controller in block diagram from GI to PI; changed header pins in note on p. 43 from JP5 to J24	Nov/07

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Audience Assumptions

This reference manual is for the person who designs computer related equipment, including but not limited to hardware and software design and implementation of the same. Ampro Computers, Inc. assumes you are qualified in designing and implementing your hardware designs and its related software into your prototype computer equipment.

Contents

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Chapter 1 About This Manual

Purpose of this Manual

This manual is for designers of systems based on the ReadyBoard™ 800 single board computer (SBC). This manual contains information that permits designers to create an embedded system based on specific design requirements.

Information provided in this reference manual includes:

- ReadyBoard 800 Specifications
- Environmental requirements
- Major integrated circuits (chips) and features implemented
- ReadyBoard 800 connector/pin numbers and definition
- BIOS Setup Utility information

Information not provided in this reference manual includes:

- Detailed chip specifications
- Internal component operation
- Internal registers or signal operations
- Bus or signal timing for industry standard busses and signals

Reference Material

The following list of reference materials may be helpful for you to complete your design successfully. Most of this reference material is also available on the Ampro web site in the Embedded Design Resource Center. The Embedded Design Resource Center was created for embedded system developers to share Ampro's knowledge, insight, and expertise gained from years of experience.

Specifications

- EPIC Specification Revision 1.0, March 22, 2004

  Web site: http://www.ampro.com/RP/EPIC_Specification_v1.0.pdf
- PC/104™ Specification Revision 2.5, November 2003
- PC/104-Plus™ Specification Revision 2.0, November 2003
- PCI-104™ Specification Revision 1.0, November 2003

  For latest revision of the PC/104, PC/104-Plus, and PCI-104 specifications, contact the PC/104 Consortium, at:

  Web site: http://www.pc104.org
- PCI™ 2.3 Specifications

  For latest revision of the PCI specifications, contact the PCI Special Interest Group Office at:

  Web site: http://www.pcisig.com
- Compact Flash Specifications Revision 3.0, December 2004

  For the latest revision of the compact flash specifications, contact the Compact Flash association at:

  Web site: http://www.CompactFlash.org

Major Integrated Circuit (IC or Chip) specifications used on the ReadyBoard 800:

- Intel® Corporation and the Pentium® M 745, Pentium M 738, Celeron® M 373, or Celeron M processors

  Web site: http://www.intel.com/design/mobile/datashts/302189.htm

  Web site: http://www.intel.com/design/mobile/datashts/303110.htm

  Web site: http://www.intel.com (Contact Intel sales for 800 MHz Celeron M)

- Intel Corporation and the chips, 82855GME and 82801DBM, used for the Graphics & Memory Hub (Northbridge) and I/O Hub (Southbridge) respectively.

  Web site: http://www.intel.com/design/chipsets/datashts/25261505.pdf

  Web site: http://www.intel.com/design/mobile/datashts/25233701.pdf

- Winbond Electronics, Corp. and the W83627HF chip used for the Super I/O controller

  Web site: Web site: http://www.winbond-usa.com/products/winbond_products/pdfs/PCIC/W83627HF_F_HG_Ga.pdf

- Intel Corporation and the 82551ER, used for the Ethernet 1 controller.

  Web site: http://www.intel.com/design/network/datashts/82551ER_ds.htm

- Intel Corporation and the 82541GI, used for the Gigabit Ethernet 2 controller.

  Web site: http://www.intel.com/design/network/datashts/82541gi_ei.pdf

NOTE	If you are unable to locate the datasheets using the links provided, go to the manufacturer's web site where you can perform a search using the chip datasheet number or name listed, including the extension, (htm for web page, pdf for files name, etc.)

Related Ampro Products

The following items are directly related to successfully using the Ampro product you have just purchased or plan to purchase. Ampro highly recommends that you purchase and utilize a ReadyBoard 800 QuickStart Kit to do your project development.

ReadyBoard 800 Support Products

- ReadyBoard 800 QuickStart Kit (QSK)

  The QuickStart Kit includes the ReadyBoard 800, DDR SODIMM memory, a cable kit, documentation, and the ReadyBoard 800 Documentation and Support Software (Doc & SW) CD-ROM.

- ReadyBoard 800 Documentation and Support Software CD-ROM

  The ReadyBoard 800 Documentation and Software (Doc & SW) CD-ROM is provided with the ReadyBoard 800 QuickStart Kit. The CD-ROM includes all of the ReadyBoard 800 documentation, including this Reference Manual and the ReadyBoard 800 QuickStart Guide in PDF format, the software utilities, board support packages, and drivers for the unique devices used with Ampro supported operating systems.

- ReadyBox™ Family

  The ReadyBox family includes a series of enclosures with varying sizes that accept all of Ampro's ReadyBoard products. These ReadyBox enclosures allow you to install your ReadyBoard product with your preferred set of options for a rapidly deployable system for OEM production volumes. The ReadyBox family provides all of the standard PC style edge connectors of the ReadyBoard products, which are accessible on the front I/O panel, including three audio connectors, and a slot for a compact flash card. Depending on the enclosure, you may add PC style connectors for two additional serial ports (4 total), two additional USB ports (4 total), and one parallel port connector. You can add up to two PC/104, PC/104-Plus, or PCI-104 expansion boards to the ReadyBox ATX and 2U enclosures. The ReadyBox ATX is powered by an internal 150 W ATX power supply and the ReadyBox 1U and 2U are powered by a AC-DC converter or a customer-specific DC power supply. A mounting location is provided for the internal 2 ½" hard disk drive and the external mounting brackets and feet are provided as accessories. Optional rack mounting hardware and an optional +12 VDC Brick power supply are provided for the ReadyBox 1U and 2U enclosures.

- ReadySystem™ Family

  The ReadySystem family is a series of high performance, low cost turnkey systems that come with a ReadyBoard 800 installed into a particular size ReadyBox enclosure with a specific size SODIMM, and a 2 ½" hard disk drive pre-loaded with one of Ampro's supported operating systems (Linux®, etc.). The ReadySystem provides all of the ReadyBoard's standard PC style connectors accessible on the front I/O panel, including three audio connectors and a slot for a compact flash card. Depending on the enclosure, you may add PC style connectors for two additional serial ports (4 total), two additional USB ports (4 total), and one parallel port connector. You can install up to two PCI-104 or PC/104-Plus expansion boards into the ReadySystem ATX and 2U enclosures. A ReadySystem comes pre-tested and ready for application loading to provide customers with the fastest possible deployment of their embedded applications. Refer to the specific ReadySystem Users Guide on the Ampro web site, or on the ReadyBoard 800 Documentation and Support Software (Doc & SW) CD-ROM for more information.

- ReadyPanel™ Family – The ReadyPanel family is a series of high performance, low cost, turnkey systems incorporating an LCD and a touch screen for a Human Machine Interface solution. All ReadyPanels come with one of Ampro's versatile ReadyBoard models in a variety of touch screen sizes pre-loaded with one of Ampro's supported operating systems (Windows® CE, etc.). The ReadyPanel includes a compact flash socket, a specific size of SODIMM memory, an Ethernet port, two serial ports, two USB ports standard, with two additional USB ports on selected models. The current models include an integrated 4-wire resistive 6.5" touch screen that displays up to 262k colors. The ReadyPanel is powered by +5 VDC (for board) and +12 VDC (for panel).

Other ReadyBoard Products

- ReadyBoard™ 700 – This EPIC single board computer (SBC) is used for high volume embedded applications and provides designers with a low cost, low-power choice of high performance Intel® 650 MHz LV Celeron, or 400 MHz Ultra Low Voltage (ULV) Celeron processors. In addition to the standard ReadyBoard features (4.5" x 6.5" form factor, PC style connectors, PC/104-Plus, +5 volt only power, etc.), the ReadyBoard 700 supports two primary IDE drives, includes one compact flash socket on secondary IDE, eight GPIO pins, four RS-232 serial ports with the RS-485/RS-422 option for two ports, dual 10/100BaseT Ethernet interfaces, four USB v1.1 ports, IrDA, and AC'97 audio ports. It also supports up to 512 MB of SDRAM in an SODIMM socket, up to 32 MB UMA of AGP 4X video with built-in LVDS, CRT, and 36-bit TFT support, and Ampro embedded BIOS extensions, such as watchdog timer, battery-free boot, a customizable splash screen, BIOS recovery, and serial console.

Other Ampro Products

- CoreModule™ Family – These complete embedded-PC subsystems on single PC/104 or PC/104-Plus form-factor (3.6"x3.8") modules feature 486, Celeron, and Celeron M CPUs. Each CoreModule includes a full complement of PC core logic functions, plus disk controllers, and serial and parallel ports. Most modules also include CRT and flat panel graphics controllers and/or an Ethernet interface. The CoreModules also come with built-in extras to meet the critical reliability requirements of embedded applications. These include onboard solid state disk compatibility, watchdog timer, smart power monitor, and Ampro embedded BIOS extensions.
- ETX Family – These high-performance, compact, rugged Computer-on-Module (COM) solutions use various x86 processors from Intel Celeron to Pentium M CPUs in an ETX Revision 2.7 form factor to plug into your custom baseboard. Each ETX module provides standard peripherals, including dual Ultra/DMA 33/66/100 IDE, floppy drive interface, PCI bus, ISA bus, serial, parallel, PS/2 keyboard and mouse interfaces, 10/100BaseT Ethernet, USB ports, Video, and AC'97 audio. ETX modules support up to 1 GB of SODIMM DRAM and come with a 50% thicker PCB, and additional features, such as watchdog timer, battery-free boot, a customizable splash screen, BIOS recovery, and serial console. Optional –40°C to +85°C operation is also available to meet your rugged application requirements.
- LittleBoard™ Family – These high-performance, highly integrated single-board computers use the EBX form factor (5.75"x8.00"), and are available with the Intel Pentium M, Celeron M, Pentium III, or Celeron processors. The EBX-compliant LittleBoard single-board computers offer functions equivalent to a complete laptop or desktop PC system, plus several expansion cards. Built-in extras to meet the critical requirements of embedded applications include onboard solid state disk capability, watchdog timer, a customizable splash screen, BIOS recovery, serial console, smart power monitor and optional –40°C to +85°C operation.
- MightyBoard™ Family – These low-cost, high-performance single-board computers (SBC) use the Mini-ITX form factor (6.75" x 6.75") and are available with Intel Celeron M and Pentium M processors. MightyBoard products offer the equivalent functions of a complete laptop or desktop PC system, including DDR memory, high performance graphics, USB 2.0, Gigabit Ethernet, plus standard PCI expansion capability in one card slot. Ampro includes additional features, such as, watchdog timer, battery-free boot, a customizable splash screen, BIOS recovery, and serial console.
- MiniModule™ Family – This line of peripheral interface modules, compliant with PC/104, PC/104-Plus, and/or PCI-104 standards (3.6"x3.8"), can be used with Ampro's CoreModule, LittleBoard, and ReadyBoard single board computers (SBCs) to expand the I/O configuration of embedded systems. Ampro's highly reliable MiniModule products add value to existing designs by adding I/O ports, such as IEEE 1394 (Firewire), or by adding support for legacy boards, such as a PCI to ISA bridge adapter.

Chapter 2 Product Overview

This introduction presents general information about the EPIC Architecture and the ReadyBoard 800 single board computer (SBC). After reading this chapter you should understand:

- EPIC Architecture
- ReadyBoard 800 architecture
- ReadyBoard 800 features
- Major components
- Connectors
- Specifications

EPIC Architecture

In 2004, five companies collaborated to fill the void between the EBX size and the PC/104 size with a new industry standard form factor (115 mm x 165 mm, or 4.5" x 6.5") called "Embedded Platform for Industrial Computing™ (EPIC)." The EPIC standard principally defines physical size, mounting hole pattern, and power connector locations. It does not specify processor type or electrical characteristics. There are recommended connector placements for serial, parallel, Ethernet, graphics, and memory expansion. This embedded SBC standard ensures that embedded system OEMs can standardize their designs and that full featured embedded computing solutions can be designed into even more space constrained environments than ever before.

The EPIC standard boasts the same highly flexible and adaptable system expansion as EBX, allowing easy and modular addition of functions such as Firewire or wireless networking not usually contained in standard product offerings. The EBX system expansion is based on popular existing industry standards, PC/104™, PC/104-Plus™, and PCI-104™. PC/104 places the ISA bus on compact 3.6" x 3.8" modules with self-stacking capability. PC/104-Plus adds the power of a PCI bus to PC/104 while retaining the basic form factor, but PCI-104 expansion cards only provide the PCI Bus to the PC/104 form factor. Using PC/104 expansion cards, an EPIC board can be easily adapted to meet a variety of embedded applications. See Figures 2-1 and 2-2.

The EPIC standard also brings stability to the mid-sized embedded board market and offers OEMs assurance that a wide range of products will be available from multiple sources – now and in the future. The EPIC specification is freely available to all interested companies, and may be used without licenses or royalties. For further technical information on the EPIC standard Rev 1.0, visit the web site at http://www.ampro.com/RP/EPIC_Specification_v1.0.pdf.

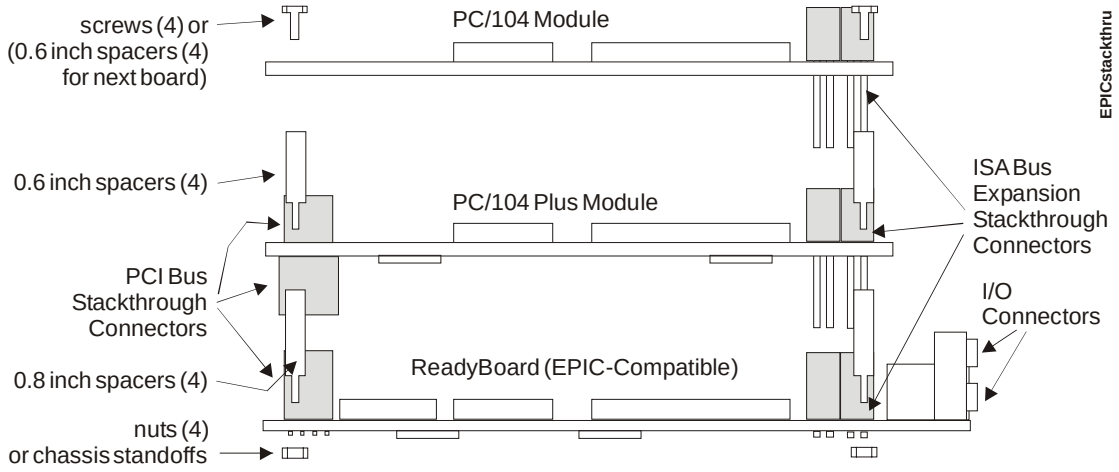


Figure 2-1. Typical ReadyBoard and PC/104 Module Stack

Product Description

The ReadyBoard 800 is a mid-sized, EPIC-compatible, affordable, high quality single-board system, which contains all the component subsystems of a PC/AT PCI motherboard plus the equivalent of several PCI expansion boards. The ReadyBoard 800 is based on one of the ultra high performance, high-integration Intel Pentium M or Celeron M processors. These processors with the matching chip set give designers a complete integration solution with a high performance embedded processor based on the EPIC form factor that conforms to the Revision 1.0 of the EPIC standard.

Each ReadyBoard 800 incorporates a Intel® 855GME chipset for the Graphics & Memory Hub (Northbridge) and I/O Hub (Southbridge) controllers. This includes the Intel 82855GME Graphics & Memory Hub, which controls the graphics and the memory interface and the Intel 82801DBM I/O Hub Controller for I/O functions. The Winbond Electronics Corp. Super I/O controller, W83627HF, adds I/O functions. Together, the Intel and Winbond chips provide four serial ports, a floppy or EPP/ECP parallel port, four USB 2.0 ports, PS/2 keyboard and mouse interfaces, an Ultra/DMA 33/66 IDE controller supporting two IDE drives and one compact flash socket, AGP 4X graphics equivalent controller, which provides CRT and LVDS flat panel video interfaces for the most popular flat panels, and an audio AC'97 CODEC on the board. The ReadyBoard 800 also supports two independent Ethernet interfaces, 10/100BaseT and 1000BaseT, and up to 1 GB of ECC or non-ECC DDR RAM in a single 200-pin SODIMM socket.

The ReadyBoard 800 can be expanded through the PCI-104 expansion bus to accept PCI-104 cards that offer compact, self-stacking, modular expandability for additional system functions. The PCI-104 bus only implements the signal set for the PCI bus and is available on the 120-pin (4 rows of 30 pins) expansion bus connector. If required for an application, the PC/104 bus, an embedded system version of the signal set provided on a desktop PC's ISA bus, can be provided by the optional Ampro MiniModule ISA expansion board. The PCI bus operates at 33 MHz clock speed and if included as an option, the ISA bus operates at 8 MHz clock speed. See Figure 2-2.

Among the many enhancements provided on the ReadyBoard 800 to ensure system operation and application versatility are a watchdog timer, serial console (remote access) support, battery-free boot, customizable splash screen, on-board high-density compact flash card socket, and ACPI support for sleep states.

The ReadyBoard 800 is particularly well suited to embedded applications by meeting the size, power consumption, temperature range, quality, and reliability demands of embedded system applications. It can be stacked with Ampro MiniModules™ or other PCI-104 compliant expansion boards, or it can be used as powerful computing engine. The ReadyBoard 800 only requires a single +5V power supply.

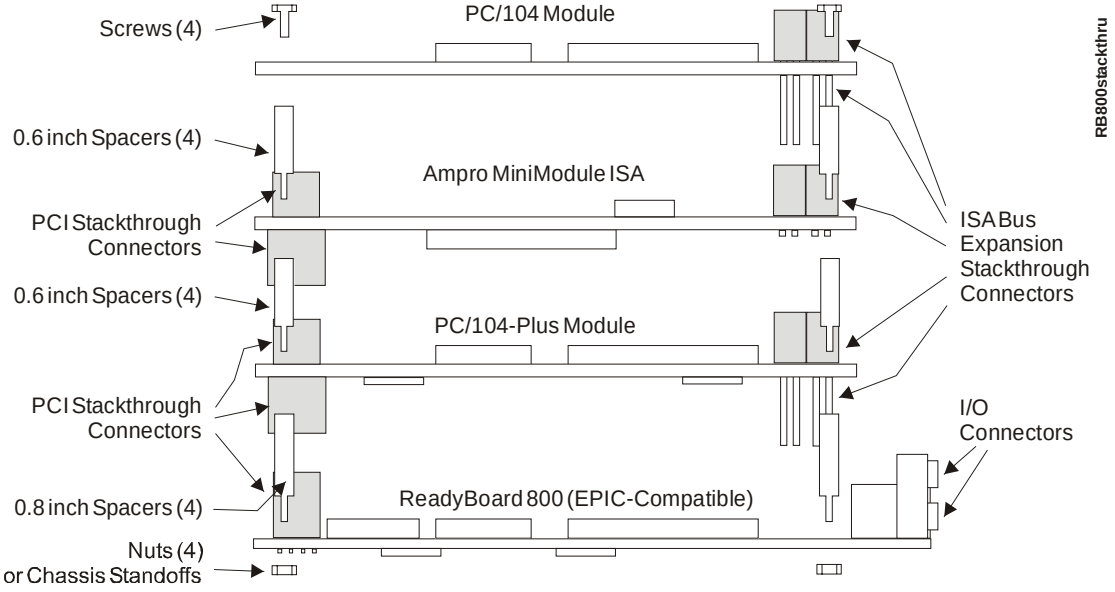


Figure 2-2. Stacking PC/104 Modules with a ReadyBoard 800

Board Features

- CPU features
  - Provides 1.8 GHz Intel Pentium M, 1.4 GHz Low Voltage (LV) Pentium M, 1.0 GHz Ultra Low Voltage (ULV) Celeron M, or 800 MHz Ultra Low Voltage (ULV) Celeron M processors
  - All processors support a Front Side Bus (FSB) of 400 MHz
- Memory
  - Provides a single standard 200-pin DDR SODIMM socket
  - Supports a single +2.5V DDR RAM SODIMM up to 1 GB
  - Supports PC2700 DDR 333 (333 Mbps, 166 MHz)
  - Provides 512 kB of flash memory
- PCI-104 Bus Interface
  - Supports PCI 2.3 standard
  - Supports 33 MHz PCI Bus speed
  - Supports optional PC/104 standard (add-on MiniModule ISA expansion board)
  - Supports PC/104 standard at 8 MHz
- IDE Interfaces
  - Provides two enhanced IDE controllers
  - Supports two IDE drives on Primary IDE and one compact flash card on Secondary IDE
  - Supports dual bus master mode
  - Supports Ultra DMA 33/66/100 modes
  - Supports ATAPI and DVD peripherals
  - Supports IDE native and ATA compatibility modes
  - Compact flash socket (Secondary IDE only)
    - Supports IDE compact flash card
    - Supports compact flash on secondary IDE bus with Master/Slave jumper
    - Supports bootable compact flash card
- Floppy/Parallel Interface
  - Shared floppy/parallel connector
  - Supports one floppy disk drive (1 standard 34-pin floppy drive)
  - Supports all standard PC/AT formats: 360 kB, 1.2 MB, 720 kB, 1.44 MB, 2.88 MB
  - Supports standard printer port
  - Supports IEEE standard 1284 protocols of EPP and ECP outputs
  - Bi-directional data lines
  - Supports 16 byte FIFO for ECP mode
- Serial Ports
  - Provides four buffered serial ports with full handshaking
  - Provides two DB9 connectors Serial 1 & 2 (COM1 & COM2)
  - Provides two serial ports Serial 3 & 4 (COM3 & COM4) through 20-pin header

- Provides 16550-equivalent controllers, each with a built-in 16-byte FIFO buffer
- Supports full modem capability on three of the four ports
- Supports RS-232 operation on all four ports
- Supports RS-485 or RS-422 operation on two ports, Serial 3 & 4 (COM3 & COM4)
- Supports programmable word length, stop bits, and parity
- Supports 16-bit programmable baud-rate generator

- USB Ports
  - Provides two root USB hubs
  - Provides four USB ports
  - Provides two standard USB connectors (USB 0 & 1) and one 10-pin header (USB 2 & 3)
  - Supports USB v2.0 and legacy v1.1 devices
  - Supports one USB floppy disk drive
  - Provides over-current shared fuses on board
- Audio interface
  - Supports AC'97 audio standard
  - Provides AC'97 CODEC
  - Provides non-amplified Stereo Line In/Out
  - Provides non-amplified MIC in (Mono)
- Ethernet Interfaces
  - Provides two fully independent Ethernet (RJ45) ports
  - Provides Intel's 82551ER and 825541GI (Gigabit) Ethernet controllers
  - Provides integrated LEDs on each port (Link/Activity and Speed)
  - Supports IEEE 802.3 10BaseT/100BaseTX compatible physical layer
  - Supports IEEE 802.3x 10BaseT/100BaseTX/1000BaseT compatible physical layer
  - Supports Auto-negotiation for speed, duplex mode, and flow control
  - Supports full duplex or half-duplex mode
  - Full-duplex mode supports transmit and receive frames simultaneously
  - Supports IEEE 802.3x flow control in full duplex mode
  - Half-duplex mode supports enhanced proprietary collision reduction mode
- Video Interfaces (CRT/LVDS)
  - Support CRT (1600 x 1200) with 64 MB UMA (Unified Memory Architecture)
  - Provides standard 15-pin VGA connector
  - Provides AGP 4X equivalent performance
  - Provides LVDS outputs (1 or 2 channels; four differential signal pairs; two 12-bit interleaved or one 24-bit non-interleaved) on 30-pin header
- Infrared Interface
  - Provides IrDA v1.1 signals on separate connector (J9)
  - Supports HPSIR and ASKIR infrared modes
  - Supports IR mode select from the Super I/O chip

- Keyboard/Mouse Interface
  - Provides PS/2 keyboard (shared with mouse) interface
  - Provides PS/2 mouse (shared with keyboard) interface
  - Provides shared over-current fuse
- Miscellaneous
  - Provides real-time clock (RTC) with replaceable battery
  - Supports battery-free boot
  - Supports external battery option
  - Provides Thermal and Voltage monitoring
  - Supports Remote Access (Serial Console or Console Redirection)
  - Provides General Purpose I/O (GPIO) capability
  - Provides SMBus header for external device connection
  - Oops! Jumper (BIOS Recovery)
  - Supports LAN Boot (PXE)
  - Supports watchdog timer (WDT)
  - Supports splash screen customization

Block Diagram

Figure 2-3 shows the functional components of the ReadyBoard 800.

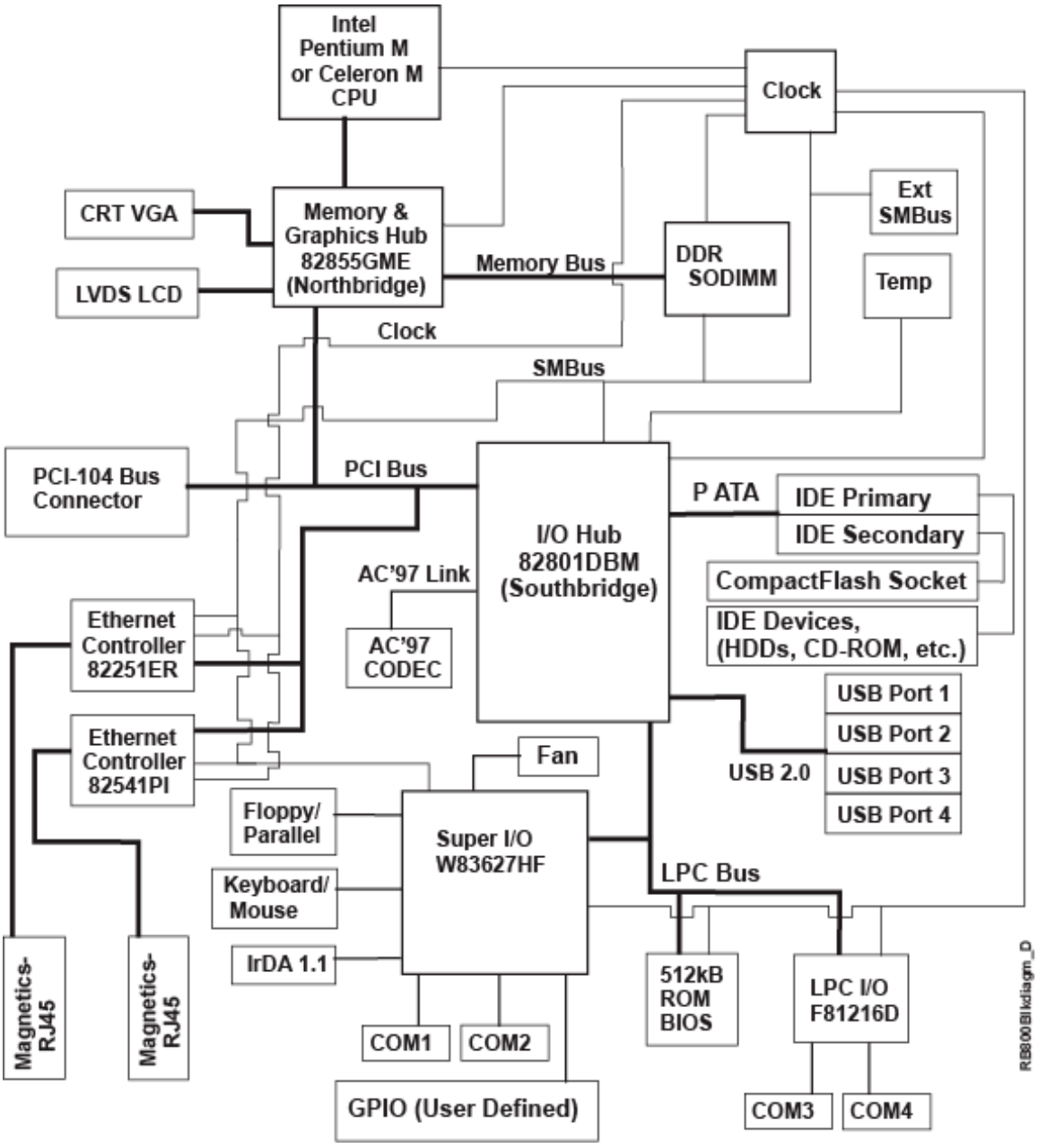


Figure 2-3. Functional Block Diagram

Major Integrated Circuits (ICs)

Table 2-1 lists the major integrated circuits (ICs or chips) on the ReadyBoard 800, including a brief description of each, and Figure 2-4 shows the location of the major chips.

Table 2-1. Major Integrated Circuit Description and Function

Chip Type	Mfg.	Model	Description	Function
CPUs (U5)	Intel	Pentium M Celeron M	1.8 GHz, LV 1.4 GHz, ULV 1.0 GHz, or ULV 800 MHz CPUs	Embedded CPU
Memory Hub (U7)	Intel	82855GME	Northbridge functions plus Video	Memory and Video
I/O Hub (U6)	Intel	82801DBM	Southbridge functions (provides some of standard I/O functions)	I/O Functions
Super I/O (U14)	Winbond Electronics, Corp.	W83627HF	Super I/O controller provides remaining standard I/O functions	I/O Functions
Ethernet Controllers (U12, U13)	Intel	82551ER 82541GI	Ethernet chips provide two independent 10/100BaseT and 1000/100/10BaseT based network channels	Ethernet Functions

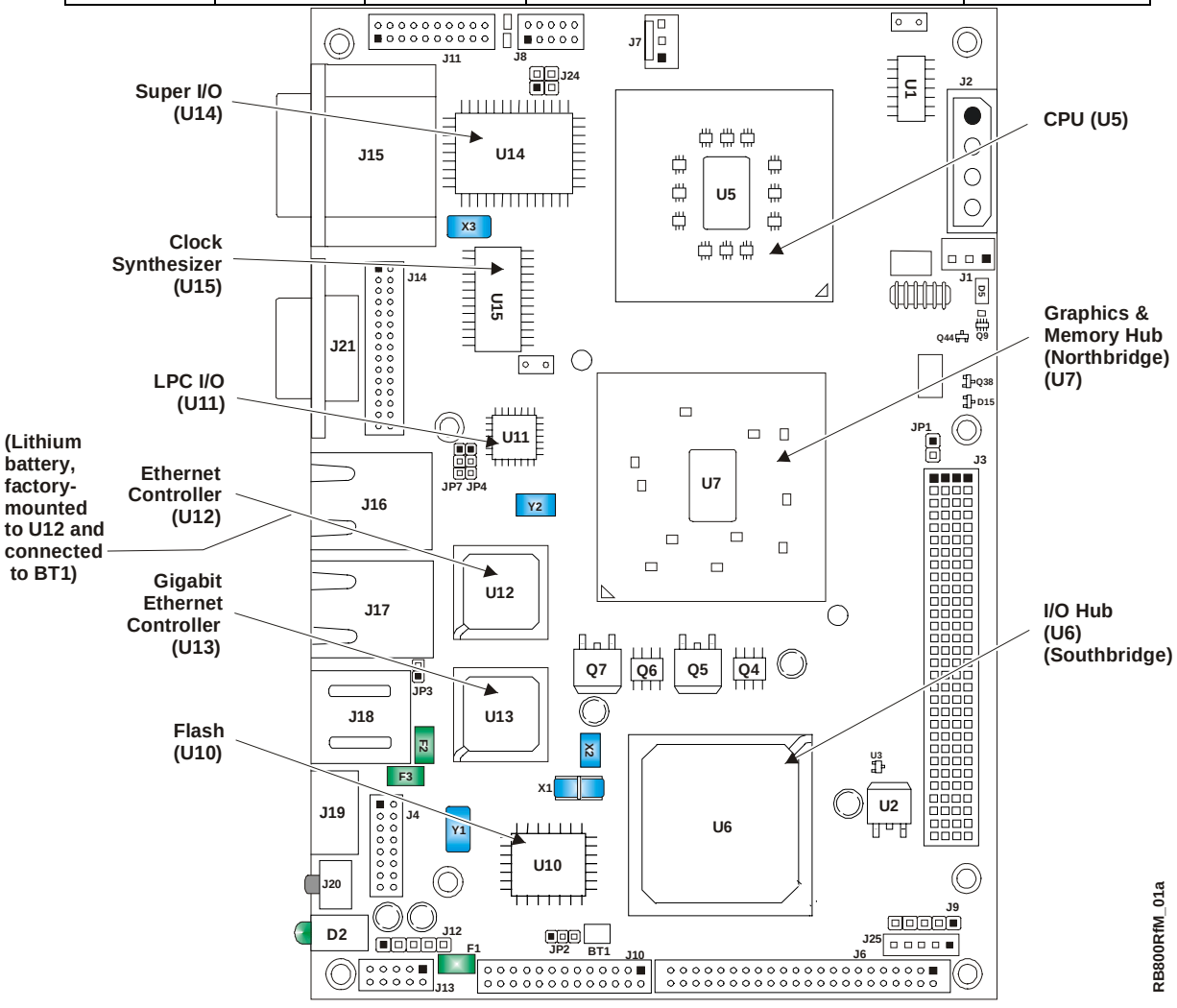


Figure 2-4. Component Location (Top view)

Connector Definitions

Table 2-2 describes the connectors shown in Figures 2-4 to 2-7. All I/O connectors use 0.1" pin spacing, where applicable, unless otherwise indicated.

Table 2-2. Connector Descriptions

Jack #	Signal/Device	Description
BT1	RTC battery (B1)	2-pin, 1.25 mm header for battery input
J1	Power On	3-pin, 2 mm header for Power On and +5V standby voltages
J2	Power In	4-pin, 5.08 mm connector for input power +5V, +12V, GND
J3	PCI-104	120-pin, 2 mm, connector for PCI bus
J4	Audio In/Out	16-pin, 2 mm connector for Line In L/R, Line Out L/R, Mic in
J6	Primary IDE	44-pin, 2 mm connector for the primary IDE interface
J7	CPU Fan	3-pin header provides +12v, tach, and ground to CPU fan.
J8	GPIO	10-pin, 2 mm header for GPIO signals
J9	IrDA	5-pin header for IrDA signals
J10	Floppy/Parallel Port	26-pin, 2 mm connector for floppy/parallel port interface
J11	Serial B	20-pin, 2 mm connector for Serial ports 3 & 4 (COM3 & COM4)
J12	Utility	5-pin header for external Battery, Reset, Speaker
J13	USB 2 & 3	10-pin, 2 mm connector provides USB2 and USB3 output
J14	Video (LVDS)	30-pin, 2 mm connector for LVDS video display
J15A/B	Serial A	9-pin dual connectors for Serial ports 1 & 2 (COM1 & COM2, DB9)
J16	Ethernet 1 + LEDs	14-pin connector for 8-pin RJ45 and LEDs for Ethernet port 1
J17	Ethernet 2 + LEDs	14-pin connector for 8-pin RJ45 and LEDs for Ethernet port 2
J18A/B	USB 0 & 1	8-pin connector for two 4-pin interfaces provide USB0 and USB1
J19	Keyboard/Mouse	6-pin, 2 mm PS/2 Keyboard/Mouse connector (dual output cable)
J21	Video (CRT VGA)	15-pin connector for output to a CRT monitor
J22	SODIMM	200-pin socket for DDR SDRAM SODIMM
J23	Compact Flash Socket	50-pin, 1.27 mm, socket accepts compact flash cards (Type I or II)
J25	SMBus	5-pin, 2 mm, SMBus header for external device connection

NOTE Ampro uses a connector/header numbering method in Chapter 3 to ease connector pin identification. For example, a 20-pin header with two rows of pins, using odd/even numbering, where pin-2 is directly across and adjacent to pin-1, is noted in this way; 20-pin, 2 rows, odd/even (1, 2). Alternately, a 20-pin connector using consecutive numbering, where pin-11 is directly across and adjacent to pin-1, is noted in this way; 20-pin, 2 rows, consecutive (1, 11). The second number in the parenthesis is always directly across from and adjacent to pin-1, with a few exceptions (PCI-104, PC/104, etc.). See Figure 2-5.

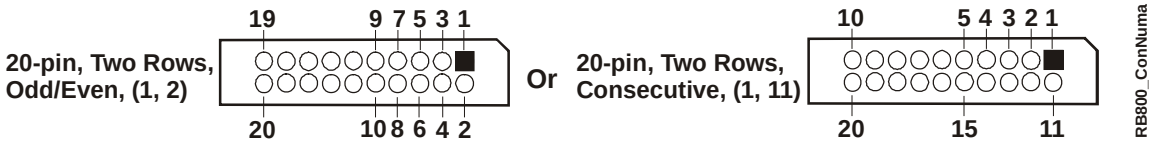


Figure 2-5. Connector Pin-Out Identifications

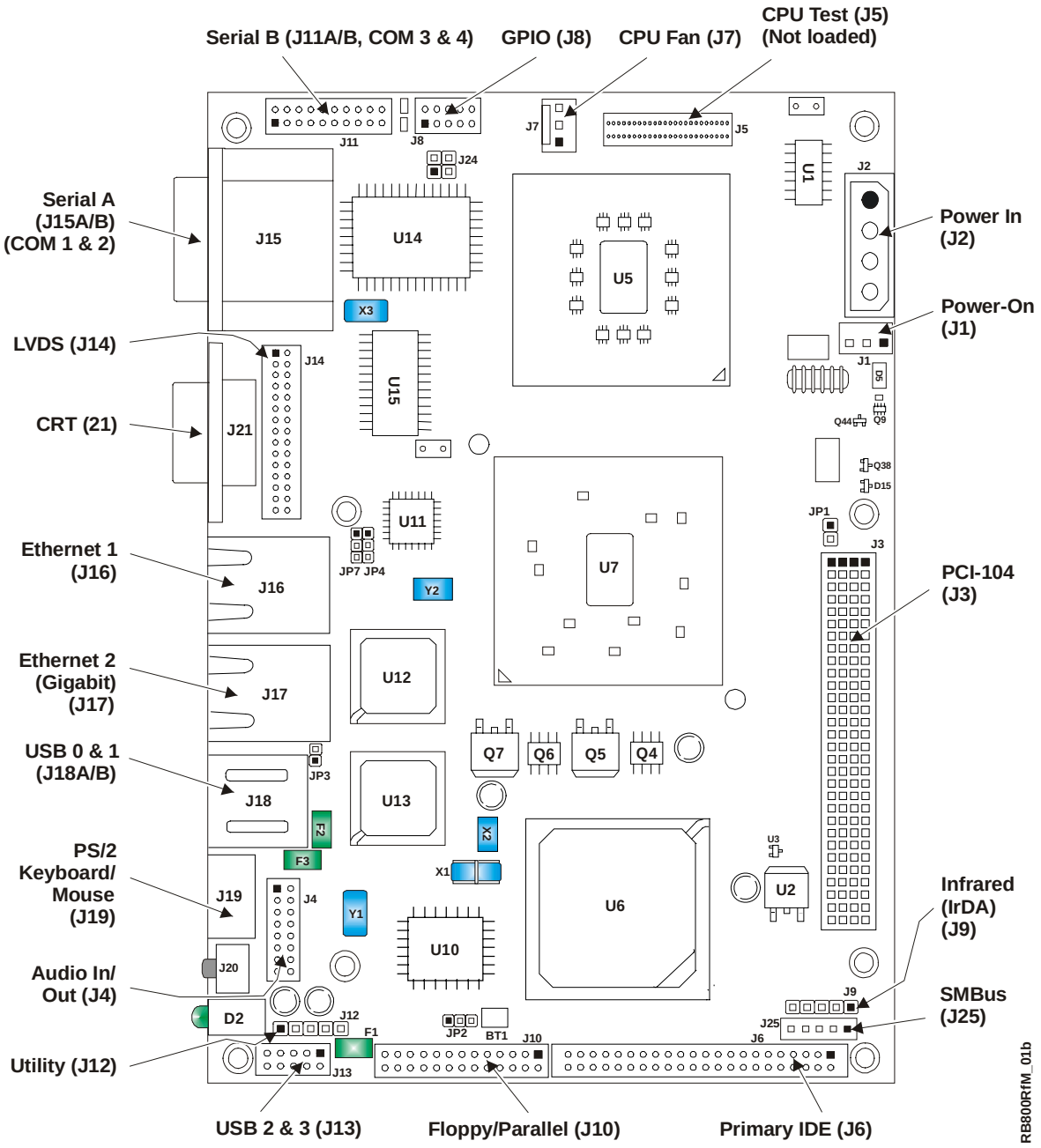


Figure 2-6. Connector Locations (Top view)

NOTE	Pin-1 is shown as a black pin (circle or square) in all connectors and jumpers in all illustrations. To comply with the PC/104, PC/104-Plus, or PCI-104 specifications, some pins in the connectors/headers are missing or have keys blocking the pins.

Jumper Definitions

Table 2-3 describes the jumpers shown in Figure 2-7. Refer to the Oops! Jumper for BIOS recovery.

Table 2-3. Jumper Settings

Jumper #	Installed/Enabled	Removed/Enabled
JP1* – ISA IRQ (SerialIRQ)	Enabled (pins 1-2)	Disabled (removed) **Default**
JP2 – CMOS Normal/Clear	Normal (pins 1-2) **Default**	Clear (Resets CMOS, pins 2-3)
JP3 – CF Master/Slave	Master (pins 1-2)	Slave (removed) **Default**
JP4 – LCD Voltage Type	Enable +3.3V (pins 1-2) **Default**	Enable +5V (pins 2-3)
JP7 – CF Voltage Select	Enable +3.3V (pins 1-2) **Default**	Enable +5V (pins 2-3)
J24 – COM3 RS485	Termination (pins 1-2)	No Termination (removed) **Default**
J24 – COM4 RS485	Termination (pins 3-4)	No Termination (removed) **Default**

NOTE * The ISA interrupts are required on pin 31 (B1) of J3 on the PCI-104 connector, when using the MiniModule ISA board. Use the ISA IRQ jumper (JP1) to enable the ISA interrupts. For full PCI-104 compatibility the jumper should be removed (default setting). Refer to MiniModule ISA manual for more information.

Ethernet LED Definitions

Tables 2-4 and 2-5 provide the LED colors and definitions for the Ethernet ports, Port 1 (J16) and Port 2 (J17) located on the ReadyBoard 800. Refer to Figures 2-6 and 2-10.

Table 2-4. Ethernet Port 1 (J16) LED Indicators

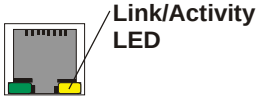
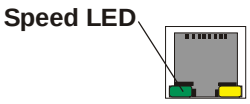
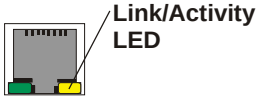
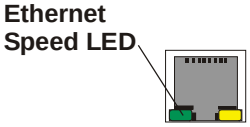
Indicator	Definition
	Link/Activity LED – This yellow LED is the activity/link indicator and provides the status of Ethernet port 1 (J16). • A steady On LED indicates a link is established. • A flashing LED indicates active data transfers.
	Speed LED – This green LED is the Speed indictor and indicates transmit or receive speed of Ethernet port 1 (J16). • A steady On LED indicates the port is at 100BaseT speed. • A steady Off LED indicates the port is at 10BaseT speed.

Table 2-5. Ethernet Port 2 (J17) LED Indicators

Indicator	Definition
	Link/Activity LED – This yellow LED is the activity/link indicator and provides the status of Ethernet port 2 (J17). • A steady On LED indicates a link is established. • A flashing LED indicates active data transfers.
	Speed LED – This green LED is the Speed indictor and indicates transmit or receive speed of Ethernet port 2 (J17). • A steady Off LED indicates the port is at 10 or 100BaseT speed. • A steady On LED indicates the port is at 1000BaseT speed.

Power/IDE LED Definitions

Table 2-6. Power/IDE Activity LED Indicators (D2)

LED #	Activity (On)	No Activity (Off)
Green LED (D2, Stack)	**Steady Green = Power On**	**Steady Off = Power Off**
Yellow LED (D2, Stack)	**Flashing Yellow = IDE activity** (IDE drive or compact flash)	**Steady Off = No IDE activity**

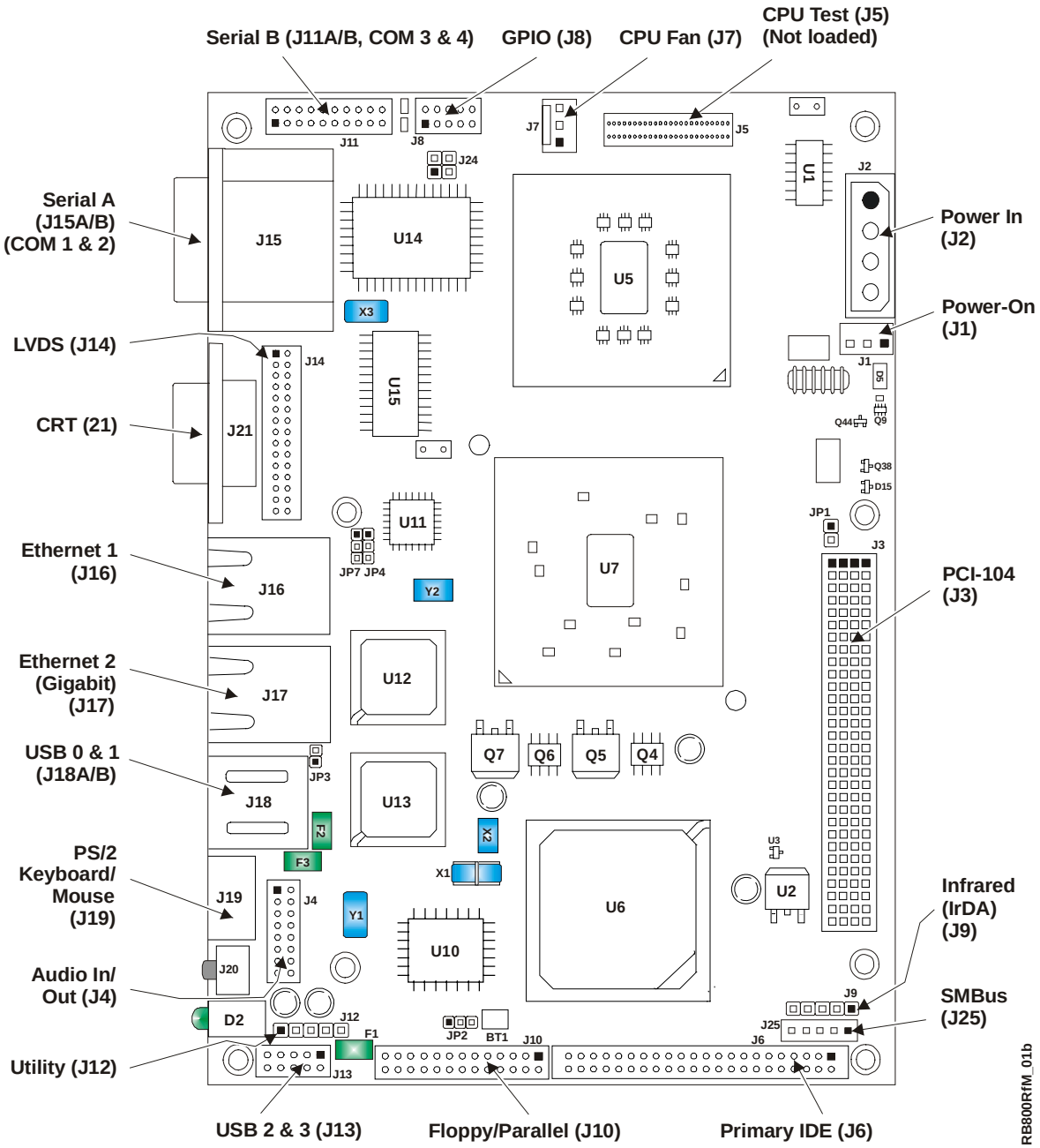


Figure 2-7. Jumper, Switch, Fuse, and LED Locations (Top view)

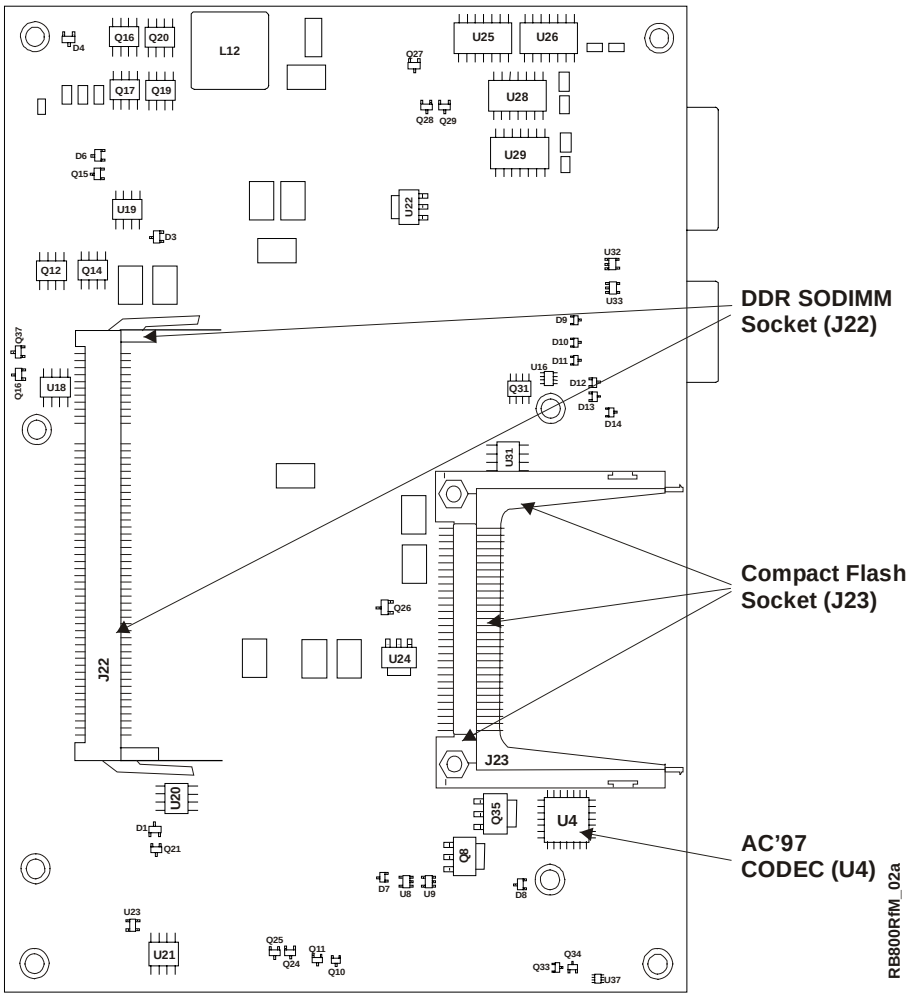


Figure 2-8. Connector and Component Locations (Bottom view)

Switch Definition

Table 2-7. Reset Switch (J20)

Component	Description
Reset Switch (J20)	4-pin, momentary push button switch

Note: The reset switch (J20) is located on the edge of the ReadyBoard 800. See Figures 2-7 and 2-10.

Additional Components

The fuses in Table 2-8 are shown in Figure 2-7.

Table 2-8. Additional Component Descriptions

Component	Description
Fuse (F1)	Auto-reset, 1.6 Amp shared fuse for USB 0 & USB 1
Fuse (F2)	Auto-reset, 1.6 Amp shared fuse for USB 2 & USB 3
Fuse (F3)	Auto-reset, 1.1 Amp shared fuse for Keyboard/Mouse protection

Specifications

Physical Specifications

Table 2-9 lists the physical dimensions of the board. Figures 2-9 and 2-10 give the mounting dimensions, including side views, and Figure 2-9 shows the pin-1 connector locations.

Table 2-9. Weight and Footprint Dimensions

Parameter	Dimensions
Weight	0.117 kg. (0.26 lb.)
Height (overall)	28.44 mm (1.12")
Width	115 mm (4.5")
Length	165 mm (6.5")
PCB Thickness	1.574 mm (0.062")

NOTE Overall height is measured from the upper board surface to the highest permanent component (at Serial A) on the upper board surface. This measurement does not include the heatsinks available for these boards. See Figure 2-10.

Power Specifications

Table 2-10 lists the ReadyBoard 800 power requirements.

Table 2-10. Power Supply Requirements

Parameter / Model	Input Type	In-rush* Current	BIT** Current
800 MHz ULV Celeron M	Regulated DC voltages	+5.0V @ 16.12A	Typical 3.31A (16.54W)
1.0 GHz ULV Celeron M	Regulated DC voltages	+5.0V @ 16.1A	Typical 3.51A (17.55W)
1.4 GHz LV Pentium M	Regulated DC voltages	+5.0V @ 16.2A	Typical 3.72A (18.58W)
1.8 GHz Pentium M	Regulated DC voltages	+5.0V @ 14.16A	Typical 3.95A (19.77W)

Notes: *In-rush measured with video, 128 MB memory, and power connected. Typically, in-rush current reflects the short duration current spike associated with charging large on-board bulk capacitance during power supply start up. However, the listed in-rush current value is the result of placing a switch on the DC output of a fully 'ramped' power supply to give a worst-case current value, which is much higher than the standard method. This in-rush value should be regarded as a maximum design guideline, not a requisite value.

**The BIT (burn in test) is conducted with 128 MB DDR SODIMM, floppy (1), IDE HDD (1), USB HDD (1), USB CD-ROM (1), keyboard, mouse, serial loopbacks (4), USB compact flash reader (1) and one card (64 MB), USB Thumb drive (1), and active Ethernet channels (2) in a Windows® XP OS environment.

Mechanical Specifications

Figures 2-9 and 2-10 show the top view and side views of the ReadyBoard 800 with the mechanical mounting dimensions.

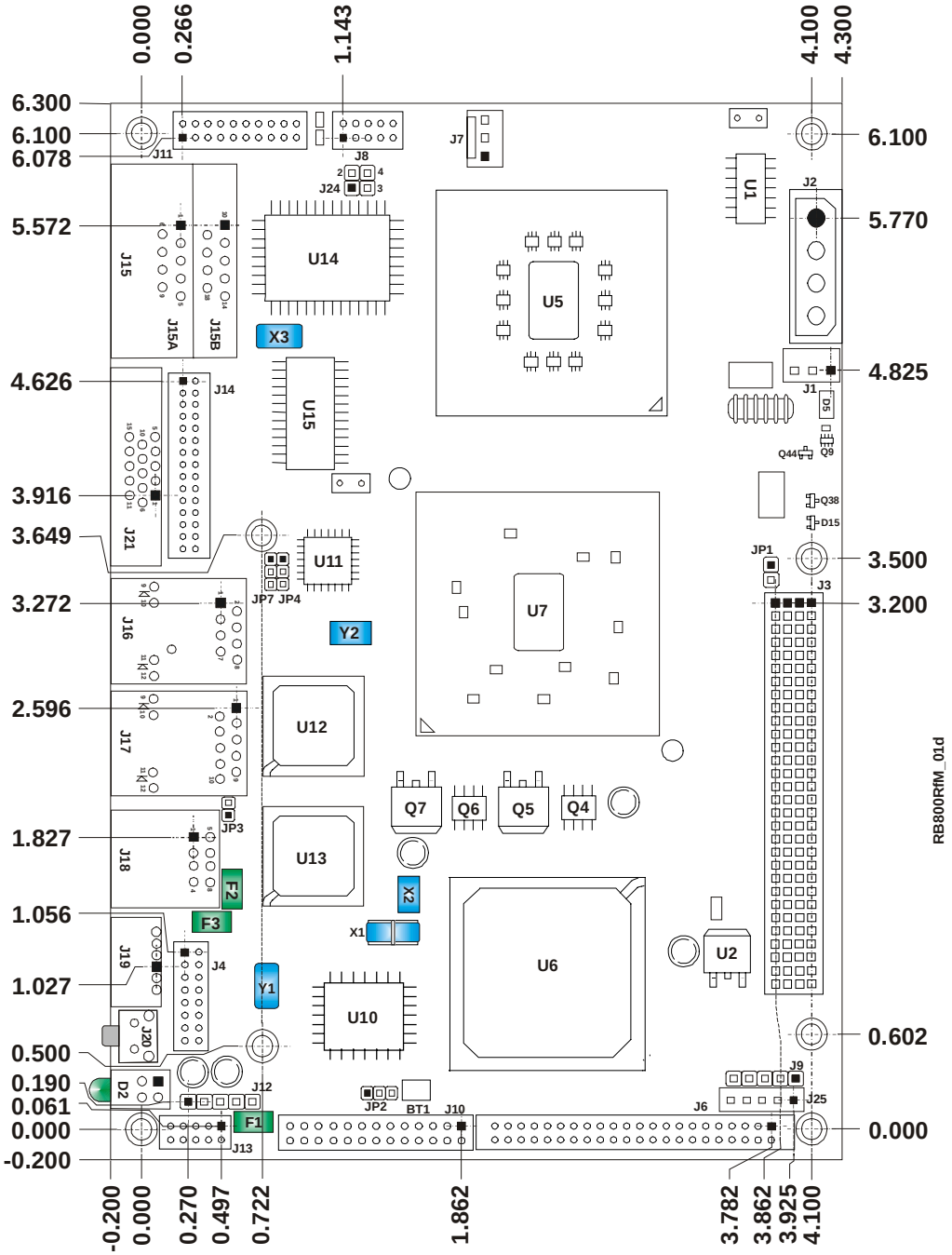


Figure 2-9. ReadyBoard 800 Dimensions (Top view)

NOTE	All dimensions are given in inches, unless otherwise specified.

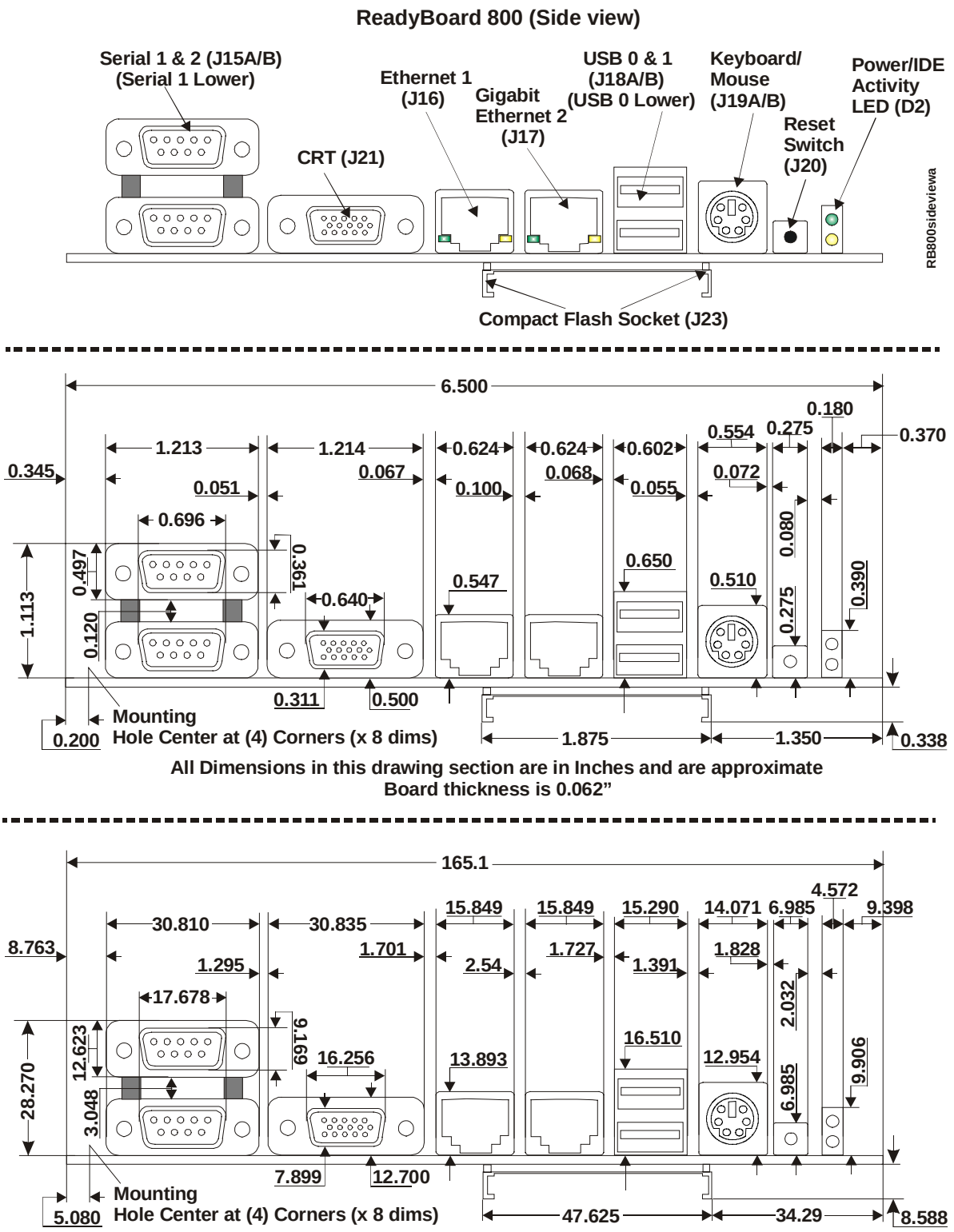


Figure 2-10. ReadyBoard 800 Panel Dimensions (Side view)

Environmental Specifications

Table 2-11 provides the most efficient operating and storage condition ranges required for this board.

Table 2-11. Environmental Requirements

Parameter	Temperature		Humidity	
Model	**Operating**	**Storage**	**Operating**	**Non-operating**
800 MHz ULV Celeron M	+0° to + 60° C (32° to + 140° F)	–20° to +75° C (–4° to +167° F)	5% to 95% relative humidity, non-condensing	5% to 95% relative humidity, non-condensing
1.0 GHz ULV Celeron M	+0° to + 60° C (32° to + 140° F)	–20° to +75° C (–4° to +167° F)	5% to 95% relative humidity, non-condensing	5% to 95% relative humidity, non-condensing
1.4 GHz LV Pentium M	+0° to + 60° C (32° to + 140° F)	–20° to +75° C (–4° to +167° F)	5% to 95% relative humidity, non-condensing	5% to 95% relative humidity, non-condensing
1.8 GHz Pentium M	+0° to + 60° C (32° to + 140° F)	–20° to +75° C (–4° to +167° F)	5% to 95% relative humidity, non-condensing	5% to 95% relative humidity, non-condensing

Thermal/Cooling Requirements

The CPU, Graphics & Memory Hub (Northbridge), I/O Hub (Southbridge), Super I/O, and voltage regulators are the sources of heat on the board. The ReadyBoard 800 is designed to operate at its maximum CPU speed of 800 MHz, 1.0 GHz, 1.4 GHz, or 1.8 GHz. All processors (except 1.8 GHz) and the Graphics & Memory Hub (Northbridge) require a heatsink, but no fan.

However, the 1.8 GHz CPU model requires a heatsink and fan. The CPU fan connector (J7) on the ReadyBoard 800 requires a +12 volt fan. The +12 volts is routed as a pass through voltage from the Power In (J2) connector to the CPU fan (J7) connector.

CAUTION	To prevent damage to the 1.8 GHz CPU, you must supply +12 volts to the Power In connector (J2) for the fan voltage on the CPU Fan connector (J7). The +12 volt fan will only operate on the +12 volt pass through voltage provided by Power In connector (J2).

Chapter 3 Hardware

Overview

This chapter discusses the chips and features of the connectors in the following order:

- CPU (U5)
- Memory (J22)
- PCI-104 (J3A, B, C, D)
- IDE Interfaces (J6)
- Compact Flash Socket (J23)
- Floppy/Parallel Interface (J10)
- Serial Interfaces (J11A/B, J15A/B)
- USB (J13A/B, J18A/B)
- Ethernet Interfaces (J16, J17)
- Audio Interface (J4)
- Video Interfaces (J14, J21)
- Miscellaneous
  - Utility Interfaces (J12)
  - Reset Switch (J20)
  - Keyboard/Mouse (J19)
  - User GPIO signals (J8)
  - Infrared (IrDA) Port (J9)
  - System Management Bus (SMBus, J25)
  - Real Time Clock (RTC)
  - Oops! Jumper (BIOS Recovery)
  - Temperature Monitoring
  - Remote Access (Serial Console)
  - Watchdog timer
- Power Interfaces (J1, J2, J7)
- Power and Sleep States

NOTE	Ampro Computers, Inc. only supports the features/options tested and listed in this manual. The main integrated circuits (chips) used in the ReadyBoard 800 may provide more features or options than are listed for the ReadyBoard 800, but some of these chip features/options are not supported on the board and may not function as specified in the chip documentation.

CPU (U5)

The ReadyBoard 800 supports four Intel processor choices; high performance standard voltage 1.8 GHz Pentium M 745, Low Voltage (LV) 1.4 GHz Pentium M 738, Ultra Low Voltage (ULV) 1.0 GHz Celeron M 373, or Low Voltage (LV) 800 MHz Celeron M.

Celeron M Processors

The Celeron M Ultra Low Voltage (ULV) processor (Dothan core) at 800 MHz has 0 kB L2 Cache on board, with a 400 MHz FSB (front side bus). The 800 MHz Celeron M processor uses 90 nm architecture and requires a heatsink, but no fan.

The Celeron M 373 Ultra Low Voltage (ULV) processor (Dothan core) at 1.0 GHz has 512 kB L2 Cache on board, with a 400 MHz FSB (front side bus). The 1.0 GHz Celeron M 373 processor uses 90 nm architecture and requires a heatsink, but no fan.

Pentium M Processors

The Pentium M 738 Low Voltage (LV) processor (Dothan core) at 1.4 GHz has 2 MB L2 Cache on board with a 400 MHz FSB (front side bus). The 1.4 GHz Pentium M 738 processor uses 90 nm architecture and requires a heatsink, but no fan.

The Pentium M 745 standard voltage processor (Dothan core) at 1.8 GHz has 2 MB L2 Cache on board with a 400 MHz FSB (front side bus). The 1.8 GHz Pentium M 745 processor uses 90 nm architecture and requires a heatsink and +12 volt fan.

NOTE	The CPU fan (J7) connector requires a +12 volt fan to operate properly. The ReadyBoard 800 provides the pass through +12 volts on the Power In (J2) connector to the CPU fan (J7) connector, the PCI-104 connector (J3), and the LVDS connector (J14).

Memory

The ReadyBoard 800 memory (storage) consists of the following elements:

- DDR RAM SODIMM
- Flash memory

DDR RAM Memory (J22)

The ReadyBoard 800 supports a single 200-pin DDR SODIMM socket.

- SODIMM socket can support up to 1 GB of memory
- PC 2700 DDR 333 (333 Mbps, 166 MHz, 6 ns)
- +2.5V DDR RAM

NOTE	Ampro recommends using PC 2700 DDR 333 (333 Mbps, 166 MHz, 6 ns), +2.5V, 200-pin, DDR RAM SODIMM for maximum performance. The ReadyBoard 800 will operate acceptably with a PC 2100 DDR 266 (266 Mbps, 133 MHz, 7.5 ns) SODIMM.

Flash Memory (U10)

There is an 8-bit wide, 512 kB flash device used for system BIOS and it is connected to the LPC Bus. The BIOS is re-programmable and the supported features are detailed in Chapter 4, BIOS Setup Utility.

Interrupt Channel Assignments

The channel interrupt assignments are listed in Table 3-1.

Table 3-1. Interrupt Channel Assignments (Typical)

Device vs IRQ No.	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Timer	D															
Keyboard		D														
Secondary Cascade			D													
COM1				O	D											
COM2				D	O											
COM3					O					O	O	D				
COM4				O						O	D	O				
Floppy							D									
Parallel						O		D								
RTC									D							
IDE Primary															D	O
IDE Secondary															O	D
Math Coprocessor														D		
PS/2 Mouse													D			
Sound Blaster						D										
PCI INTA	Automatically Assigned															
PCI INTB	Automatically Assigned															
PCI INTC	Automatically Assigned															
PCI INTD	Automatically Assigned															
USB	Automatically Assigned															
VGA	Automatically Assigned															
Ethernet	Automatically Assigned															

Legend: D = Default, O = Optional Refer also to the IRQs listed in Chapter 4, BIOS Setup Utility.

NOTE	The IRQs for the Ethernet, Video, and USB are automatically assigned by the BIOS Plug and Play logic. Local IRQs assigned during initialization can not be used by external devices.

Memory Map

The following table provides the common PC/AT memory allocations. Memory below 000500h is used by the BIOS. Refer to Table 3-2.

Table 3-2. Memory Map

Base Address	Function
00000000h - 0009FFFFh	Conventional Memory
000A0000h - 000AFFFFh	Graphics Memory
000B0000h - 000B7FFFh	Mono Text Memory
000B8000h - 000BFFFFh	Color Text Memory
000C0000h - 000CFFFFh	Standard Video BIOS
000E0000h - 000FFFFFh	System BIOS Area (Storage and RAM Shadowing)
00100000h - 04000000h	Extended Memory (If onboard VGA is enabled, then the amount of memory assigned is subtracted from extended memory)
FFF80000h - FFFFFFFFh	System Flash

I/O Address Map

Table 3-3 list the I/O address map.

Table 3-3. I/O Address Map

Address (hex)	Subsystem
000-00F	Primary DMA Controller
020-021	Master Interrupt Controller
040-043	Programmable Interrupt Timer (Clock/Timer)
060-06F	Keyboard Controller
070-07F	CMOS RAM, NMI Mask Reg, RT Clock
080-09F	DMA Page Registers
092	Fast A20 gate and CPU reset
094	Motherboard enable
102	Video subsystem register
0A0-0BF	Slave Interrupt Controller
0C0-0DF	Slave DMA Controller #2
0F0-0FF	Math Coprocessor
170-177	Secondary IDE Hard Disk Controller
1F0-1F8	Primary IDE Hard Disk Controller
201	Watchdog Timer (WDT)
278-27F	Parallel Printer
2E8-2FF	Serial Port 4 (COM4)
2F8-2FF	Serial Port 2 (COM2)
378-37F	Parallel port (Standard and EPP)
3C0-3DF	VGA
3E8-3EF	Serial Port 3 (COM3)
3F0-3F7	Floppy Disk Controller
3F8-3FF	Serial Port 1 (COM1)
778-77A	Parallel Port (ECP Extensions) (Port 378+400)
CF8-CFF	PCI bus Configuration Address and Data

PCI-104 Interface (J3)

The PCI-104 expansion interface uses a 120-pin (30x4) 2 mm connector. This connector carries all of the appropriate PCI signals operating at clock speeds up to 33 MHz. The I/O Hub (82801DBM), integrates a PCI arbiter that supports up to four devices with three external PCI masters. This interface header accepts stackable modules and is located on the top of the board.

Table 3-4 provides the PCI-104 pins/signals and descriptions for 120-pins, 4 individual rows, consecutive order (B1, A1, C1, D1), with 2 mm pin spacing.

Table 3-4. PCI-104 Pin/Signal Descriptions (J3)

Pin #	Signal	Input/ Output	Description
1 (A1)	KeyNC		Key Not Connected
2 (A2)	VI/O		Reference Voltage – +5 volts
3 (A3)	AD05	T/S	PCI Address and Data Bus Line 5 – These address and data signal lines (0-31) are multiplexed. A bus transaction consists of an address followed by one or more data cycles.
4 (A4)	C/BE0*	T/S	PCI Bus Command/Byte Enable 0 – This signal line is one of four signal lines. These signal lines are multiplexed, so that during the address cycle, the command is defined and during the data cycle, the byte enable is defined.
5 (A5)	GND		Ground
6 (A6)	AD11	T/S	PCI Address and Data Bus Line 11 – See Pin-3 for more information.
7 (A7)	AD14	T/S	PCI Address and Data Bus Line 14 – See Pin-3 for more information.
8 (A8)	+3.3V		+3.3 volts ±5%
9 (A9)	SERR*	O/D	System Error – This signal is for reporting address parity errors.
10 (A10)	GND		Ground
11 (A11)	STOP*	S/T/S	Stop – This signal indicates the currently selected device is requesting the current transaction be stopped by the master.
12 (A12)	+3.3V		+3.3 volts ±5%
13 (A13)	FRAME*	S/T/S	PCI Bus Frame access – This signal is driven by the current master to indicate the start of a transaction and will remain active until the final data cycle
14 (A14)	GND		Ground
15 (A15)	AD18	T/S	PCI Address and Data Bus Line 18 – See Pin-3 for more information.
16 (A16)	AD21	T/S	PCI Address and Data Bus Line 21 – See Pin-3 for more information.
17 (A17)	+3.3V		+3.3 volts ±5%
18 (A18)	IDSEL0	In	Initialization Device Select 0 – This signal line is one of four signal lines and is used as the chip-select signal during configuration.
19 (A19)	AD24	T/S	PCI Address and Data Bus Line 24 – See Pin-3 for more information.
20 (A20)	GND		Ground

Pin #	Signal	Input/ Output	Description
21 (A21)	AD29	T/S	PCI Address and Data Bus Line 29 – See Pin-3 for more information.
22 (A22)	+5V		+5.0 volts ±5%
23 (A23)	REQ0*	T/S	Bus Request 0 – This signal line is one of three signal lines. These signals indicate the device desires use of the bus to the arbitrator.
24 (A24)	GND		Ground
25 (A25)	GNT1*	T/S	Grant 1 – This signal line is one of three grant lines and these indicate access has been granted to the requesting device (PCI Masters).
26 (A26)	+5V		+5.0 volts ±5%
27 (A27)	CLK2	In	PCI clock 2 – This signal line is one of four clock signal lines and these provide the timing outputs for four external PCI devices and the timing for all transactions on the PCI bus.
28 (A28)	GND		Ground
29 (A29)	+12V		+12.0 volts ±5%
30 (A30)	NC		Not connected - Reserved
31 (B1)	SERIRQ		Serial IRQ – This signal line provides the serial IRQs for the MiniModule ISA expansion board if used. See Table Notes.
32 (B2)	AD02	T/S	PCI Address and Data Bus Line 2 – See Pin-3 for more information.
33 (B3)	GND		Ground
34 (B4)	AD07	T/S	PCI Address and Data Bus Line 7 – See Pin-3 for more information.
35 (B5)	AD09	T/S	PCI Address and Data Bus Line 9 – See Pin-3 for more information.
36 (B6)	VI/O		Reference Voltage – +5 volts
37 (B7)	AD13	T/S	PCI Address and Data Bus Lines 13 – See Pin-3 for more information.
38 (B8)	C/BE1*	T/S	PCI Bus Command/Byte Enable 1 – See Pin-4 for more information.
39 (B9)	GND		Ground
40 (B10)	PERR*		Parity Error – This signal is for reporting data parity errors.
41 (B11)	+3.3V		+3.3 volts ±5%
42 (B12)	TRDY*	S/T/S	Target Ready – This signal indicates the selected device's ability to complete the current cycle of transaction. Both IRDY* and TRDY* must be asserted to terminate a data cycle.
43 (B13)	GND		Ground
44 (B14)	AD16	T/S	PCI Address and Data Bus Line 16 – See Pin-3 for more information.
45 (B15)	+3.3V		+3.3 volts ±5%
46 (B16)	AD20	T/S	PCI Address and Data Bus Lines 20 – See Pin-3 for more information.
47 (B17)	AD23	T/S	PCI Address and Data Bus Line 23 – See Pin-3 for more information.
48 (B18)	GND		Ground

Pin #	Signal	Input/ Output	Description
49 (B19)	C/BE3*	T/S	PCI Bus Command/Byte Enable 3 – See Pin-4 for more information.
50 (B20)	AD26	T/S	PCI Address and Data Bus Line 26 – See Pin-3 for more information.
51 (B21)	+5V		+5.0 volts ±5%
52 (B22)	AD30	T/S	PCI Address and Data Bus Line 30 – See Pin-3 for more information.
53 (B23)	GND		Ground
54 (B24)	REQ2*	T/S	Bus Request 2 – This signal indicates a device desires use of the bus sent to the arbitrator. This request line is not available when the MiniModule ISA board is used. See Notes.
55 (B25)	VI/O		Reference Voltage – +5 volts
56 (B26)	CLK0	In	PCI clock 0 – See Pin 27 for more information
57 (B27)	+5V		+5.0 volts ±5%
58 (B28)	INTD*	O/D	Interrupt D – This signal is used to request interrupts only for multi-function devices.
59 (B29)	INTA*	O/D	Interrupt A – This signal is used to request an interrupt.
60 (B30)	REQ#3		
61 (C1)	+5V		+5.0 volts ±5%
62 (C2)	AD01	T/S	PCI Address and Data Bus Line 1 – See Pin-3 for more information.
63 (C3)	AD04	T/S	PCI Address and Data Bus Lines 4 – See Pin-3 for more information.
64 (C4)	GND		Ground
65 (C5)	AD08	T/S	PCI Address and Data Bus Line 8 – See Pin-3 for more information.
66 (C6)	AD10	T/S	PCI Address and Data Bus Line 10 – See Pin-3 for more information.
67 (C7)	GND		Ground
68 (C8)	AD15	T/S	PCI Address and Data Bus Line 15 – See Pin-3 for more information.
69 (C9)	SB0*		Snoop Backoff – Tied to +5 volts through 10k ohm resistor.
70 (C10)	+3.3V		+3.3 volts ±5%
71 (C11)	LOCK*	S/T/S	Lock – This signal indicates an operation that may require multiple transactions to complete
72 (C12)	GND		Ground
73 (C13)	IRDY*	S/T/S	Initiator Ready – This signal indicates the master's ability to complete the current data cycle of the transaction
74 (C14)	+3.3V		+3.3 volts ±5%
75 (C15)	AD17	T/S	PCI Address and Data Bus Line 17 – See Pin 3 for more information.
76 (C16)	GND		Ground

Pin #	Signal	Input/ Output	Description
77 (C17)	AD22	T/S	PCI Address and Data Bus Line 22 – See Pin-3 for more information.
78 (C18)	IDSEL1		Initialization Device Select 1 – See Pin-18 for more information
79 (C19)	VI/O		Reference Voltage – +5 volts
80 (C20)	AD25	T/S	PCI Address and Data Bus Line 25 – See Pin-3 for more information.
81 (C21)	AD28	T/S	PCI Address and Data Bus Line 28 – See Pin-3 for more information.
82 (C22)	GND		Ground
83 (C23)	REQ1*	T/S	Bus Request 1 – See Pin-23 for more information.
84 (C24)	+5V		+5.0 volts ±5%
85 (C25)	GNT2*	T/S	Grant 2 – See Pin-25 for more information. This signal line is reserved for the MiniModule ISA expansion board. See Notes.
86 (C26)	GND		Ground
87 (C27)	CLK3	In	PCI clock 3 – See Pin-27 for more information
88 (C28)	+5V		+5.0 volts ±5%
89 (C29)	INTB*	O/D	Interrupt B – This signal is only used to request interrupts for multi-function devices.
90 (C30)	GNT3*		
91 (D1)	AD00	T/S	PCI Address and Data Bus Line 0 – See Pin-3 for more information.
92 (D2)	+5V		+5.0 volts ±5%
93 (D3)	AD03	T/S	PCI Address and Data Bus Lines 3 – See Pin-3 for more information.
94 (D4)	AD06	T/S	PCI Address and Data Bus Lines 6 – See Pin-3 for more information.
95 (D5)	GND		Ground
96 (D6)	NC		Not Connected (M66EN)
97 (D7)	AD12	T/S	PCI Address and Data Bus Line 12 – See Pin-3 for more information.
98 (D8)	+3.3V		+3.3 volts ±5%
99 (D9)	PAR	T/S	PCI bus Parity bit – This signal is the even parity bit on AD[31:0] and C/BE[3:0]*.
100 (D10)	SDONE		Snoop Done – Tied to +5v through 10k ohm resistor
101 (D11)	GND		Ground
102 (D12)	DEVSEL*	S/T/S	Device Select – This signal is driven by the target device when its address is decoded.
103 (D13)	+3.3V		+3.3 volts ±5%
104 (D14)	C/BE2*		PCI Bus Command/Byte Enable 2 – See Pin-4 for more information.
105 (D15)	GND		Ground

Pin #	Signal	Input/ Output	Description
106 (D16)	AD19	T/S	PCI Address and Data Bus Line 19 – See Pin-3 for more information.
107 (D17)	+3.3V		+3.3 volts ±5%
108 (D18)	IDSEL2		Initialization Device Select 2 – See Pin-18 for more information.
109 (D19)	IDSEL3		Initialization Device Select 3 – See Pin-18 for more information.
110 (D20)	GND		Ground
111 (D21)	AD27	T/S	PCI Address and Data Bus Line 27 – See Pin-3 for more information.
112 (D22)	AD31	T/S	PCI Address and Data Bus Line 31 – See Pin-3 for more information.
113 (D23)	VI/O		Reference Voltage – +5 volts
114 (D24)	GNT0*	T/S	Grant 0 – See Pin 25 for more information.
115 (D25)	GND		Ground
116 (D26)	CLK1	In	PCI clock 1 – See Pin-27 for more information
117 (D27)	GND		Ground
118 (D28)	RST*	In	PCI bus reset – This signal is an output signal to reset the entire PCI Bus. This signal will be asserted during system reset
119 (D29)	INTC*	O/D	Interrupt C – This signal is used to request interrupts only for multi-function devices.
120 (D30)	NC		Not Connected

Notes: The shaded area denotes power or ground. The signals marked with * = Negative true logic.

The Input/Output signals in this table refer to the input/output signals listed in the PCI Local Bus Manual, Revision 2.3, Chapter 2, paragraph 2.1, Signal definitions. The following terms or acronyms are used in this table:

- In – Input is standard input only signal
- Out – Totem Pole output is a standard active driver
- T/S – Tri-State is a bi-directional input output pin
- S/T/S – Sustained Tri-State is an active low tri-state signal driven by one and only one agent at a time
- O/D – Open Drain allows multiple devices to share as a wire-OR.

NOTE One request signal (pin 54 or B24, REQ2) and one grant line (pin 85 or C25, GNT2) are not available to other cards/devices when the MiniModule ISA expansion board is used. These signal lines are reserved for the MiniModule ISA board, if jumper JP1 is enabled. The MiniModule ISA board provides the optional PC/104 bus (ISA bus) interface.

IDE Interface (J6)

The ReadyBoard 800 provides one primary IDE connector (J6) for two IDE devices and one compact flash socket (J23) on the secondary IDE controller.

The I/O Hub (Southbridge) EIDE interface logic supports the following features:

- Transfer rate up to 100 Mbps
- Increased reliability using Ultra DMA 33/66/100 transfer protocols
- Supports ATAPI and DVD compliant devices
- PIO IDE transfers as fast as 14 Mbps
- Single Bus Master EIDE
- Supports two IDE drives on primary interface and one compact flash card on the secondary IDE

Table 3-5 describes the primary IDE pins/ signals for the IDE 44-pin, 2 rows, odd/even (1, 2) with 2 mm pin spacing.

Table 3-5. Primary IDE Interface Pin/Signal Descriptions (J6)

Pin #	Signal	Description
1	RESET*	Reset – Low active hardware reset (RSTDRV inverted)
2	GND	Ground
3	PDD7	Primary Disk Data 7 – These signals (0 to 15) provide the disk data signals.
4	PDD8	Primary Disk Data 8 – See pin-3 (PDD7) for more information.
5	PDD6	Primary Disk Data 6 – See pin-3 (PDD7) for more information.
6	PDD9	Primary Disk Data 9 – See pin-3 (PDD7) for more information.
7	PDD5	Primary Disk Data 5 – See pin-3 (PDD7) for more information.
8	PDD10	Primary Disk Data 10 – See pin-3 (PDD7) for more information.
9	PDD4	Primary Disk Data 4 – See pin-3 (PDD7) for more information.
10	PDD11	Primary Disk Data 11 – See pin-3 (PDD7) for more information.
11	PDD3	Primary Disk Data 3 – See pin-3 (PDD7) for more information.
12	PDD12	Primary Disk Data 12 – See pin-3 (PDD7) for more information.
13	PDD2	Primary Disk Data 2 – See pin-3 (PDD7) for more information.
14	PDD13	Primary Disk Data 13 – See pin-3 (PDD7) for more information.
15	PDD1	Primary Disk Data 1 – See pin-3 (PDD7) for more information.
16	PDD14	Primary Disk Data 14 – See pin-3 (PDD7) for more information.
17	PDD0	Primary Disk Data 0 – See pin-3 (PDD7) for more information.
18	PDD15	Primary Disk Data 15 – See pin-3 (PDD7) for more information.
19	GND	Ground
20	NC-Key	Not Connected - Key pin plug
21	PDREQ	Primary DMA Channel Request – Used for DMA transfers between host and drive (direction of transfer controlled by DIOR* and DIOW*). Also used in an asynchronous mode with DMACK*. Drive asserts IDRQ0 when ready to transfer or receive data.
22	GND	Ground

Pin #	Signal	Description
23	PDIOW*	Primary Device I/O Write Strobe – Strobe signal for write functions. Negative edge enables data from a register or data port of the drive onto the host data bus. Positive edge latches data at the host.
24	GND	Ground
25	PDIOR*	Primary I/O Read Strobe – Strobe signal for read functions. Negative edge enables data from a register or data port of the drive onto the host data bus. Positive edge latches data at the host.
26	GND	Ground
27	PIORDY	Primary I/O Channel Ready – When negated extends the host transfer cycle of any host register access when the drive is not ready to respond to a data transfer request. High impedance if asserted.
28	PCSEL	Primary Cable Select – Tied to ground through 470 ohm resistor.
29	PDDACK*	Primary DMA Channel Acknowledge – Used by the host to acknowledge data has been accepted or data is available. Used in response to DMARQ assertion.
30	GND	Ground
31	IRQ14	Interrupt Request 14 – Asserted (IRQ14) by drive when it has pending interrupt (PIO transfer of data to or from the drive to the host).
32	NC	Not connected
33	PDA1	Primary IDE ATA Disk Address 1– Used (0 to 2) to indicate which byte in the ATA command block or control block is being accessed.
34	PD33/66	UDMA 33/66 Sense – Senses which DMA mode to use for IDE devices.
35	PDA0	Primary IDE ATA Disk Address 0 – See pin-33 (PDA1) for more information.
36	PDA2	Primary IDE ATA Disk Address 2 – See pin-33 (PDA1) for more information.
37	PDCS1*	Primary Chip Select 1 – Used to select the host-accessible Command Block Register.
38	PDCS3*	Primary Chip Select 3 – Used to select the host-accessible Command Block Register.
39	IDEACT*	IDE Activity – Indicates EIDE activity to yellow IDE LED (D5) on card edge.
40	GND	Ground
41	+5V	+5 volts +/-5%
42	+5V	+5 volts +/-5%
43	GND	Ground
44	NC	Not connected

Notes: The shaded area denotes power or ground. The signals marked with * = Negative true logic.

Compact Flash Socket (J23)

The board contains a compact flash socket, which allows for the insertion of a compact flash card. The compact flash card acts as a standard IDE Drive and is connected to the Secondary IDE bus. If a compact flash card is installed, it is the only device using the secondary IDE bus. A jumper is used to select the Master/Slave mode. Refer to Table 2-3, Jumper Settings for more information.

NOTE	You may use compact flash cards (Type I or II) from commercial vendors, but some compact flash cards do not support DMA or UDMA transfers. Consult the ReadyBoard 800 Hardware Release Notes and your compact flash card vendor for DMA or UDMA compatibility.

Table 3-6 provides the signals and descriptions for a standard compact flash socket, 50-pin, 2 rows, consecutive (1, 26) with 1.27 mm (0.050") pin spacing.

Table 3-6. Compact Flash Interface Pin/Signal Descriptions (J23)

Pin #	Signal	Description
1	GND	Ground
2	SDD3	Secondary Disk Data 3 – These signals (D0-D15) carry the Data, Commands, and Status between the host and the controller. D0 is the LSB of the even Byte of the Word. D8 is the LSB of the odd Byte of the Word. All Task File operations occur in byte mode on the low order bus D0-D7, while all data transfers are 16 bit using D0-D15 to provide the disk data signals.
3	SDD4	Secondary Disk Data 4 – Refer to SDD3 on pin-2 for more information.
4	SDD5	Secondary Disk Data 5 – Refer to SDD3 on pin-2 for more information.
5	SDD6	Secondary Disk Data 6 – Refer to SDD3 on pin-2 for more information.
6	SDD7	Secondary Disk Data 7 – Refer to SDD3 on pin-2 for more information.
7	SDCS1*	Secondary Chip Select 1 – This signal, along with SDCS3*, select the card and indicate when a byte or word operation is being performed. This signal accesses the even byte or odd byte of the word depending on A0 and SDCS3*.
8, 10	NC	Not connected
9	GND	Ground
11, 12	NC	Not connected
13	VCC	Voltage Pin – This voltage is determined by CF Voltage Select jumper (JP7). Pins 1-2 = +3.3V or pins 2-3 = +5V.
14, 15	NC	Not connected
16, 17	NC	Not connected
18	SDA2	Secondary Address select 2 – One of three signals (0 – 2) used to select one of eight registers in the Task File. The host grounds all remaining address lines.
19	SDA1	Secondary Address select 1 – Refer to A2 on pin-18 for more information.
20	SDA0	Secondary Address select 0 – Refer to A2 on pin-18 for more information.
21	SDD0	Secondary Disk Data 0 – Refer to SDD3 on pin-2 for more information.
22	SDD1	Secondary Disk Data 1 – Refer to SDD3 on pin-2 for more information.
23	SDD2	Secondary Disk Data 2 – Refer to SDD3 on pin-2 for more information.
24	NC	Not connected (IOCS16*)

Pin #	Signal	Description
25, 26	CD2, CD1	Card Detect 1 & 2 – Connected through 100k ohm resister to +5 VDC, when no CF card installed. A low (ground) on either pin causes an Or Gate to switch placing VCC on CF voltage pins. Refer to pins -13, -36, -38.
27	SDD11	Secondary Disk Data 11 – Refer to SDD3 on pin-2 for more information.
28	SDD12	Secondary Disk Data 12 – Refer to SDD3 on pin-2 for more information.
29	SDD13	Secondary Disk Data 13 – Refer to SDD3 on pin-2 for more information.
30	SDD14	Secondary Disk Data 14 – Refer to SDD3 on pin-2 for more information.
31	SDD15	Secondary Disk Data 15 – Refer to SDD3 on pin-2 for more information.
32	SDCS3*	Secondary Chip Select 3 – This signal, along with SDCS1*, selects the compact flash card and indicates to the card when a byte or word operation is being performed. This signal always accesses the odd byte of the word.
33, 40	NC	Not Connected (VS1*, VS2*)
34	SDIOR*	Secondary Device I/O Read/Write Strobe – This signal is generated by the host and gates the I/O data onto the bus from the compact flash card when the card is configured to use the I/O interface.
35	SDIOW*	Secondary Device I/O Read/Write Strobe – This signal is generated by the host, and clocks the I/O data onto the Card Data bus into the compact flash card controller registers when the card is configured to use the I/O interface. The clock occurs on the negative to positive edge of the signal (trailing edge).
36, 38	VCC	Voltage Pin – Refer to pin-13 for more information.
37	IRQ15	Interrupt Request 15 – IRQ 15 is asserted by drive (CF) when it has a pending interrupt (PIO transfer of data to or from the drive to the host).
39	MASTER*	Master/Slave – This pin determines the Master or Slave configuration of the compact flash by the jumper (JP3) setting. When this pin is grounded (jumper inserted), this device is configured as Master. When this pin is open (jumper removed), this device is configured as Slave (Default).
41	IDERST*	Secondary IDE Reset – This input signal is the active low hardware reset from the host. If this pin goes high, it is used as the reset signal. This pin is driven high at power-up, causing a reset, and if left high will cause another reset.
42	SDIORDY	Secondary Device I/O-DMA Channel Ready – When negated, extends the host transfer cycle of any host register access when the drive is not ready to respond to a data transfer request. High impedance if asserted.
43	SDREQ	Secondary DMA Request – Used for DMA data transfers between the host and device.
44	SDDACK*	Secondary DMA Acknowledge – Asserted by host in response to DMA request to initiate DMA transfers.
45	IDE LED2	IDE Activity – Indicates CF activity to yellow IDE LED (D5) on board edge.
46	CF2	CF2 (UDMA 33/66 Sense) – Senses the DMA mode for the compact flash.
47	SDD8	Secondary Disk Data 8 – Refer to SDD3 on pin-2 for more information.
48	SDD9	Secondary Disk Data 9 – Refer to SDD3 on pin-2 for more information.
49	SDD10	Secondary Disk Data 10 – Refer to SDD3 on pin-2 for more information.
50	GND	Ground

Notes: The shaded area denotes power or ground. The signals marked with * = Negative true logic.

Floppy/Parallel Interface (J10)

The Super I/O controller (W83627HF) provides the floppy controller and the parallel port controller. The floppy controller and the parallel port controller share the same output connector (J10) on the board and the device selection is made in the BIOS Setup Utility.

- Floppy Port Controller only supports one floppy drive, in the standard formats, such as 360 kB, 720 kB, 1.2 MB, 1.44 MB, or 2.88 MB drives.
- Parallel Port controller supports standard parallel, Bi-directional, ECP and EPP protocols.

NOTE	Due to the multiplexed nature of the signals for the floppy and parallel ports, you can only connect one of these devices at a time. Refer to Chapter 4, BIOS Setup Utility later in this manual when selecting the floppy or parallel device in the BIOS Setup Utility. A reboot is necessary for the change of BIOS settings to take affect.

Table 3-7 describes the floppy/parallel port (J10) pin/signals with 26-pins, 2 rows, consecutive (1, 14) with 2 mm pin spacing.

Table 3-7. Floppy/Parallel Interface Pin/Signal Descriptions (J10)

Pin #	Signal	Description
1	Strobe*	Parallel Strobe* – This is an output signal used to strobe data into the printer. I/O pin in ECP/EPP mode.
2	PD0	Parallel Port Data 0 – These pins (0 to 7) provide parallel port data signals.
	INDEX*	Floppy Index – Detects head positioned over the beginning of a track.
3	PD1	Parallel Port Data 1 – See pin-2 (PD0) for more information.
	TRK0*	Floppy Track 0 – Detects when head is positioned over track 0.
4	PD2	Parallel Port Data 2 – See pin-2 (PD0) for more information.
	WPRT*	Floppy Write Protect – Senses if diskette is write protected.
5	PD3	Parallel Port Data 3 – See pin-2 (PD0) for more information.
	RDATA*	Floppy Read Data – Raw serial bit stream from the drive for read operations.
6	PD4	Parallel Port Data 4 – See pin-2 (PD0) for more information.
	DSKCHG*	Floppy Disk Change – Senses when drive door is open or the diskette has been changed since the last drive selection.
7	PD5	Parallel Port Data 5 – See pin-2 (PD0) for more information.
8	PD6	Parallel Port Data 6 – See pin-2 (PD0) for more information.
9	PD7	Parallel Port Data 7 – See pin-2 (PD0) for more information.
10	ACK*	Parallel Acknowledge * – This is a status output signal from the printer. A Low State indicates it has received the data and is ready to accept new data.
	DS1*	Floppy Drive Select 1 – Select drive 1.
11	BUSY	Parallel Busy – This is a status output signal from the printer. A High State indicates the printer is not ready to accept data.
	MTR1*	Floppy Motor Control 1 – Select motor on drive 1.
12	PE	Parallel Paper End – This is a status output signal from the printer. A High State indicates it is out of paper.
	WDATA*	Floppy Write Data – Encoded data to the drive for write operations.

Pin #	Signal	Description
13	PSLCT	Printer Select – This is a status output signal from the printer. A High State indicates it is selected and powered on.
	WGATE*	Floppy Write Enable – Drive signal to enable current flow in the write head.
14	AFD*	Parallel Auto Feed* – This is a request signal into the printer to automatically feed one line after each line is printed.
	DRVEN0*	Floppy Drive Density Select Bit 0
15	ERR*	Parallel Error – This is a error status output signal from the printer. A Low State indicates an error condition on the printer.
	HDSEL*	Floppy Head Select – Selects the side for Read/Write operations (0 = side 1, 1 = side 0)
16	PINIT*	Printer Initialize* – This signal is used to Initialize printer. Output in standard mode, I/O in ECP/EPP mode.
	DIR*	Floppy Direction – Direction of head movement (0 = inward motion, 1 = outward motion).
17	SLIN	Parallel Select In – This output signal to the printer is used to select the printer. I/O pin in ECP/EPP mode.
	STEP*	Floppy Step – Low pulse for each track-to-track movement of the head.
18	GND	Ground
19	GND	Ground
20	GND	Ground
21	GND	Ground
22	GND	Ground
23	GND	Ground
24	GND	Ground
25	GND	Ground
26	NC	Not Connected

Notes: The shaded area denotes power or ground. The signals marked with * = Negative true logic.

Serial Interfaces (J15A/B, J11A/B)

The ReadyBoard supports 4 independent serial ports, using two separate chips. The Super I/O controller (W83627HF) provides Serial ports 1 and 2 through the Serial A DB9 connectors (J15A/B) and the I/O Hub (82801DBM) provides serial ports 3 and 4 through Serial B connector (J11A/B). The four serial ports support the following features:

- Four individual 16550-compatible UARTs
- Programmable word length, stop bits and parity
- 16-bit programmable baud rate generator
- Interrupt generator
- Loop-back mode
- Four individual 16-bit FIFOs
- Serial A supports ports 1 and 2 using the Super I/O Controller
  - Serial Port 1 (COM1) supports RS-232 and full modem support
  - Serial Port 2 (COM2) supports RS-232, and full modem support
- Serial B supports ports 3 and 4 using the I/O Hub (Southbridge)
  - Serial Port 3 (COM3) supports RS-232/RS-485/RS-422 and full modem support
  - Serial Port 4 (COM4) supports RS-232/RS-485/RS-422 and modem support

NOTE	The RS-232/RS-485/RS-422 modes are selected in BIOS Setup Utility under the submenu, Super I/O Configuration in the Advanced menu screen for Serial ports 3 (COM3) and 4 (COM4). However, the RS-232 mode is the default (Standard) for any serial port. RS-485 mode termination is selected with jumper J24, pins 1-2 (COM3), and pins 3-4 (COM4), when the RS-485 mode is selected in BIOS Setup Utility. Refer to Table 2-3 for more information.

To implement the two-wire RS-485 mode on either serial port, you must tie the equivalent pins together for each port.

For example; on Serial Port 3, tie pin 3 (RX3-) to 5 (TX3-) and pin 4 (TX3+) to 6 (RX3+) at the Serial B interface connector (J11) as shown in Figure 3-1. As an alternate, tie pin 2 to 3 and pin 7 to 8 at the DB9 serial connector for Serial Port 3 as shown in Figure 3-1. Refer also to the following tables for the specific pins for the other ports and connectors. The RS-422 mode uses a four-wire interface and does not require tying pins together, but you must select RS-485 in BIOS Setup Utility.

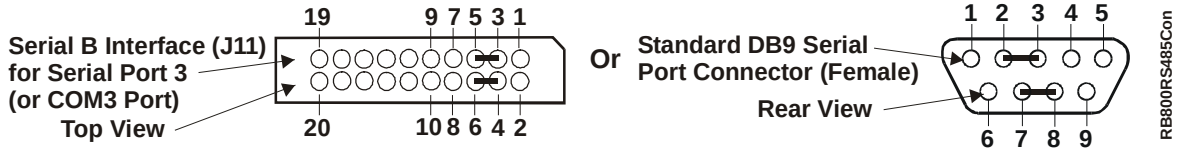


Figure 3-1. RS-485 Serial Port Implementation

Tables 3-8 and 3-9 list the pins and corresponding signals for the Serial A interface connector (J15A/B, Serial Ports 1 and 2) and Table 3-10 list the pins and corresponding signals for the Serial B interface connector (J11A/B, Serial Ports 3 and 4). Both Serial A DB9 connectors use 9-pin consecutive (1, 6) and the Serial B connector uses 10-pins, 2 rows, odd/even (1, 2) with 2 mm pin spacing as shown in Figure 3-1.

Serial A Interface (J15A/B)

Table 3-8. Serial A (Serial 1) Interface Pin/Signal Descriptions (J15A)

Pin #	Signal	Description
1	DCD1*	Data Carrier Detect 1 – Indicates external serial device is detecting a carrier signal (i.e., a communication channel is currently open). In direct connect environments, this input is driven by DTR1 as part of the DTR/DSR handshake.
2	RXD1	Receive Data 1 – Serial port 1 receive data in
3	TXD1	Transmit Data 1 – Serial port 1 transmit data out
4	DTR1*	Data Terminal Ready 1 – Indicates serial port is powered, initialized, and ready. Used as hardware handshake with DSR1 for overall readiness to communicate.
5	GND	Ground
6	DSR1*	Data Set Ready 1 – Indicates external serial device is powered, initialized, and ready. Used as hardware handshake with DTR1 for overall readiness.
7	RTS1*	Request To Send 1 – Indicates serial port is ready to transmit data. Used as hardware handshake with CTS1 for low level flow control.
8	CTS1*	Clear To Send 1 – Indicates external serial device is ready to receive data. Used as hardware handshake with RTS1 for low level flow control.
9	RI1*	Ring Indicator 1 – Indicates external serial device is detecting a ring condition. Software initiates operation to answer and open the communications channel.

Notes: The shaded area denotes power or ground. The signals marked with * = Negative true logic.

Table 3-9. Serial A (Serial 2) Interface Pin/Signal Descriptions (J15B)

Pin #	Signal	Description
1	DCD2*	Data Carrier Detect 2 – Indicates external serial device is detecting a carrier signal (i.e., a communication channel is currently open). In direct connect environments, this input is driven by DTR2 as part of the DTR/DSR handshake.
2	RXD2	Receive Data 2 – Serial port receive data in.
3	TXD2	Transmit Data 2 – Serial port transmit data out.
4	DTR2*	Data Terminal Ready 2 – Indicates serial port is powered, initialized, and ready. Used as hardware handshake with DSR2 for overall readiness to communicate.
5	GND	Ground
6	DSR2*	Data Set Ready 2 – Indicates external serial device is powered, initialized, and ready. Used as hardware handshake with DTR2 for overall readiness.
7	RTS2*	Request To Send 2 – Indicates serial port is ready to transmit data. Used as hardware handshake with CTS2 for low level flow control.
8	CTS2*	Clear To Send 2 – Indicates external serial device is ready to receive data. Used as hardware handshake with RTS2 for low level flow control.
9	RI2*	Ring Indicator 2 – Indicates external serial device is detecting a ring condition. Software initiates operation to answer and open the communications channel.

Notes: The shaded area denotes power or ground. The signals marked with * = Negative true logic.

Serial B Interface (J11A/B)

Table 3-10. Serial B Interface Pin/Signal Descriptions (J11A/B)

Pin #	Pin # DB9	Signal	Description
A1	1 (COM3)	DCD3*	Data Carrier Detect 3 – Indicates external serial device is detecting a carrier signal (i.e., a communication channel is currently open). In direct connect environments, this input is driven by DTR3 as part of the DTR/DSR handshake.
A2	6	DSR3*	Data Set Ready 3 – Indicates external serial device is powered, initialized, and ready. Used as hardware handshake with DTR3 for overall readiness.
A3	2	RXD3	Receive Data 3 – Serial port 3 receive data in.
		RX3-	RX3 Negative – If in RS-485 or RS-422 mode, this pin is Receive Data 3 -.
A4	7	RTS3*	Request To Send 3 – Indicates serial port is ready to transmit data. Used as hardware handshake with CTS3 for low level flow control.
		TX3+	TX3 Positive – If in RS-485 or RS-422 mode, this pin is Transmit Data 3 +.
A5	3	TXD3	Transmit Data 3 – Serial port 3 transmit data out.
		TX3-	TX3 Negative – If in RS-485 or RS-422 mode, this pin is Transmit Data 3 -.
A6	8	CTS3*	Clear To Send 3 – Indicates external serial device is ready to receive data. Used as hardware handshake with RTS3 for low level flow control.
		RX3+	RX3 Positive – If in RS-485 or RS-422 mode, this pin is Receive Data 3 +.
A7	4	DTR3*	Data Terminal Ready 3 – Indicates serial port is powered, initialized, and ready. Used as hardware handshake with DSR3 for overall readiness to communicate.
A8	9	RI3*	Ring Indicator 3 – Indicates external serial device is detecting a ring condition. Software initiates operation to answer and open the communications channel.
A9	5	GND	Ground
A10	NC	NC	Not connected/Key
B11	1 (COM4)	DCD4*	Data Carrier Detect 4 – Indicates external serial device is detecting a carrier signal (i.e., a communication channel is currently open). In direct connect environments, this input is driven by DTR4 as part of the DTR/DSR handshake.
B12	6	DSR4*	Data Set Ready 4 – Indicates external serial device is powered, initialized, and ready. Used as hardware handshake with DTR4 for overall readiness.
B13	2	RXD4	Receive Data 4 – Serial port 4 receive data in.
		RX4-	RX4 Negative – If in RS-485 or RS-422 mode, this pin is Receive Data 4 -.
B14	7	RTS4*	Request To Send 4 – Indicates serial port is ready to transmit data. Used as hardware handshake with CTS4 for low level flow control.
		TX4+	TX4 Positive – If in RS-485 or RS-422 mode, this pin is Transmit Data 4 +.
B15	3	TXD4	Transmit Data 4 – Serial port transmit data out.
		TX4-	TX4 Negative – If in RS-485 or RS-422 mode, this pin is Transmit Data 4 -.
B16	8	CTS4*	Clear To Send 4 – Indicates external serial device is ready to receive data. Used as hardware handshake with RTS4 for low level flow control.
		RX4+	RX4 Positive – If in RS-485 or RS-422 mode, this pin is Receive Data 4 +.

Pin #	Pin # DB9	Signal	Description
B17	4	DTR4*	Data Terminal Ready 4 – Indicates serial port is powered, initialized, and ready. Used as hardware handshake with DSR4 for overall readiness.
B18	9	NC	Not connected (RI)
B19	5	GND	Ground
B20	NC	NC	Not connected

Notes: The shaded area denotes power or ground. RS-232 signals are listed first followed by RS-485/RS-422. The signals marked with * = Negative true logic.

USB Interfaces (J18A/B, J13A/B)

The I/O Hub (82801DBM) provides the USB solution for both legacy UHCI controllers and EHCI controller (USB 2.0) support. The I/O Hub (Southbridge) contains port-routing logic that determines which controller (UHCI or EHCI) handles the USB data signals. The PC style (or Standard) connector (J18A/B) provides two of the four USB ports (USB0 and USB1). The other two USB ports share a single 10-pin header (J13A/B) on the board.

USB 2.0 Support

The I/O Hub contains an Enhanced Host Controller Interface (EHCI) compliant host controller, which supports up to 4 high-speed USB 2.0 Specification compliant root ports. The higher speed USB 2.0 specification allows data transfers up to 480 Mbps using the same pins as the 4 Full-speed/Low-speed USB UHCI ports. The I/O Hub port-routing logic determines which of the controllers (UHCI or the EHCI) processes the USB signals.

- One EHCI host controller for all four USB ports on connectors (J18A/B, and/or J13A/B)
- Supports USB v2.0 Specification
- Over-current fuses, located on the board, where USB0 and USB1 share a single fuse (F1) and USB2 and USB3 share a single fuse (F2). See Table 2-8.

Legacy USB Support

The I/O Hub supports two USB Universal Host Controller Interfaces (UHCI) and each Host Controller includes a root hub with two USB ports each, for a total of 4 USB ports. The USB Legacy features implemented on the USB ports include the following:

- One root hub and two USB ports on connector (J18A/B)
- One root hub and two USB ports on connector (J13A/B)
- Supports USB v.1.1 and UHCI v.1.1 with integrated physical layer transceivers
- Supports improved arbitration latency for UHCI controllers
- UHCI controllers support Analog Front End (AFE) embedded cell instead of USB I/O buffers to allow for USB High-speed signaling rates
- Over-current fuses, located on the board, are used on all four USB ports

Primary USB0 and USB1 (J18A/B)

Table 3-11. USB 1 & 2 Interface Pin/Signal Descriptions (J18A/B)

Pin #	Signal	Description
1	VCC	USB Voltage – +5V through sharedfuse (F1)
2	USBP0-	Universal Serial Bus Port 0 Data Negative
3	USBP0+	Universal Serial Bus Port 0 Data Positive
4	GND	Ground
5	VCC	USB Voltage – +5V through shared fuse (F1)
6	USBP1-	Universal Serial Bus Port 1 Data Negative
7	USBP1+	Universal Serial Bus Port 1 Data Positive
8	GND	Ground

Note: The shaded area denotes power or ground.

Secondary USB2 and USB3 (J13A/B)

Table 3-12 describes USB 2 & 3, J13A/B at 10-pins, 2 rows, odd/even (1, 2) with 2 mm pin spacing.

Table 3-12. USB 2 & 3 Interface Pin/Signal Descriptions (J13A/B)

Pin #	Signal	Description
1, 2	VCC	USB Voltage – +5V through sharedfuse (F2)
3	USBP2-	Universal Serial Bus Port 2 Data Negative
4	USBP3-	Universal Serial Bus Port 3 Data Negative
5	USBP2+	Universal Serial Bus Port 2 Data Positive
6	USBP3+	Universal Serial Bus Port 3 Data Positive
7, 8, 9, 10	GND	Ground

Note: The shaded area denotes power or ground.

Ethernet Interfaces (J16, J17)

The Ethernet solution is provided by two Intel Ethernet controllers, Gigabit 82541GI (in GI, PI, or EI versions) and 82551ER for Port 2 and Port 1 respectively. Both controllers consist of a Media Access Controller (MAC) and a physical layer (PHY) combined into a single component solution.

Gigabit Ethernet Controller

The Intel® 82541GI Gigabit Ethernet Controller is 32-bit wide, PCI 2.3 compliant controller capable of transmitting and receiving data rates of 1000 Mbps, 100 Mbps, or 10 Mbps. The 82541GI's gigabit MAC design fully integrates the physical layer circuitry to provide a standard IEEE 802.3 Ethernet interface for 1000BaseT, 100BaseTX, and 10BaseT applications (802.3, 802.3u, and 802.3ab).

The 82541GI controller delivers high performance, PCI bus efficiency, with wide internal data paths to eliminate performance bottlenecks by efficiently handling large address and data words. The controller includes advanced interrupt handling features to limit PCI bus traffic and a PCI interface that maximizes the use of bursts for efficient bus usage. This controller caches up to 64 packet descriptors in a single burst with a large 64 kByte on-chip packet buffer to maintain superior performance with efficient PCI bandwidth use, as available PCI bandwidth changes. In addition, using hardware acceleration, the controller offloads tasks from the host controller, such as TCP/UDP/IP checksum calculations and TCP segmentation. The 82541GI Gigabit Ethernet controller supports or provides the following features:

- Low-latency transmit and receive queues to prevent waiting periods or buffer overflow
- Supports caches of 64 packet descriptors in a signal burst to provide efficient PCI bandwidth use
- Supports programmable host memory receive buffers (256 Bytes to 16 kBytes) and cache line sizes (16 to 256 Bytes)
- Supports wide optimized internal data paths for low latency data handling and superior DMA transfer rates
- Supports 64 kByte configurable Transmit and Receive FIFO buffers
- Supports simple programming model with descriptor ring transmit and receive management hardware
- Supports jumbo frames of 16 kByte transmit and receive packets
- Supports maximized system performance and throughput with interrupt reduction of transmit and receive operations
- Full duplex or half-duplex support at 10 Mbps, 100 Mbps, and 1000 Mbps
- Supports 1000BaseT 4-wire pairs and 10BaseT/100BaseT 2-wire pairs
- IEEE 802.3x 10BaseT/100BaseT/1000BaseT compatible physical layer to wire transformer
- IEEE 802.3ab Auto-Negotiation support, includes speed, duplex, and flow control
- IEEE 802.3ab PHY compliance and compatibility with Category-5 twisted pair cabling
- Implements latest DSP architecture with digital adaptive equalization, echo cancellation, and crosstalk cancellation to achieve high performance in noisy environments (high electrical/signal interference impairment)
- Supports transmit and receive IP, TCP, and UDP checksum offloading capabilities for lower CPU utilization
- Supports Transmit TCP segmentation and advanced packet filtering
- Supports system monitoring with industry standard consoles (SNMP and RMON statistic counters)
- Supports remote network management capabilities through DMI 2.0 and SNMP software (SDG 3.0, WfM 2.0, and PC2001 compliance)
- Supports a RJ-45 connector with magnetics integrated into connector

- Supports four-pair, 100 ohm, Category 5 UTP (Unshielded Twisted Pair) wiring

Tables 3-13 describes the pin-outs and signals of Gigabit Ethernet port, Ethernet Port 2.

Table 3-13. Ethernet Port 2 Pin/Signal Descriptions (J17)

Pin #	Signal	Description
1	MDI0+	Media Dependent Interface [0] – In MDI* configuration (1000BaseT), MDI[0]+/- corresponds to BI_DA+/-, and in MDI-X* configuration, MDI[0]+/- corresponds to BI_DB+/-. In MDI configuration (10BaseT or 100BaseT-TX), MDI[0]+/- is used for transmit pair, and in MDI-X configuration, MDI[0]+/- is used for the receive pair.
2	MDI0-	
3	MDI1+	Media Dependent Interface [1] – In MDI configuration (1000BaseT), MDI[1]+/- corresponds to BI_DB+/-, and in MDI-X configuration, MDI[1]+/- corresponds to BI_DA+/-. In MDI configuration (10BaseT or 100BaseT-TX), MDI[1]+/- is used for transmit pair, and in MDI-X configuration, MDI[1]+/- is used for the receive pair.
6	MDI1-	
4	MDI2+	Media Dependent Interface [2] – In MDI configuration (1000BaseT), MDI[2]+/- corresponds to BI_DC+/-, and MDI-X configuration, MDI[2]+/- corresponds to BI_DD+/-. The 10BaseT or 100BaseT-TX are not used in this MDI pair.
5	MDI2-	
7	MDI3+	Media Dependent Interface [3] – In MDI configuration (1000BaseT), MDI[3]+/- corresponds to BI_DD+/-, and MDI-X configuration, MDI[3]+/- corresponds to BI_DC+/-. The 10BaseT or 100BaseT-TX are not used in this MDI pair.
8	MDI3-	
CT	CTap	Center Tap Ground – Goes to ground through 75 ohm resistor and 1.0 nF capacitor.
11	Speed	Speed LED – This signal line is shared with 1000BaseT and 100BaseT. The 10BaseT speed is indicated when no indication is seen for any activity.
12, 14	VCC3	LED Power – This voltage (+3.3 volts) is for plus side of both LEDs.
13	Link	Link/Activity LED – This signal indicates a Link is established or Activity is occurring over the port.
15, 16	GND	Shield Ground

Notes: The shaded area denotes power or ground. * MDI (medium dependent interface) is an Ethernet port connection that allows network hubs or switches to connect to other hubs or switches without a crossover cable. A medium dependent interface is also referred to as an MDI port or an uplink port. **MDI-X (or MDIX), short for medium dependent interface crossover (the "X" representing "crossover"), is an Ethernet port connection that allows networked end stations (i.e., PCs or workstations) to connect to each other using a crossover cable. MDIX is also referred to as an MDIX port.

10/100BaseT Ethernet Controller

Ethernet Port 1 uses an Intel 82551ER Fast Ethernet, 32-bit PCI controller chip and consists of both the Media Access Controller (MAC) and the physical layer (PHY) combined into a single component solution. The 82551ER is a 32-bit PCI controller that features enhanced scatter-gather bus mastering capabilities, which enables the 82551ER to perform high-speed data transfers over the PCI bus. The 82551ER bus master capabilities enable the component to process high-level commands and perform multiple operations, thereby off-loading communication tasks from the system CPU.

- Backward software compatible to the 8255x family
- Chained memory structure
- Full duplex or half-duplex support
- Full duplex support at 10 Mbps and 100 Mbps
- In half-duplex mode, performance is enhanced by a proprietary collision reduction mechanism.
- IEEE 802.3 10BaseT/100BaseT compatible physical layer to wire transformer
- Provides two LEDs for speed and link & activity status
- Data transmission with minimum interframe spacing (IFS).
- IEEE 802.3u Auto-Negotiation support
- 3 kB transmit and 3 kB receive FIFOs (helps prevent data underflow and overflow)
- IEEE 802.3x auto-negotiation support for speed and duplex operation
- IEEE 802.3x 100BASE-TX flow control support
- Improved dynamic transmit chaining with multiple priorities transmit queue
- Supports a RJ-45 connector with magnetics integrated into the RJ-45 connector.

Tables 3-14 describes the pin-outs and signals of standard Ethernet port, Ethernet Port 1.

Table 3-14. Ethernet Port 1 Pin/Signal Descriptions (J16)

Pin #	Signal	Description
1	TX2+	Analog Twisted Pair Ethernet Transmit Differential Pair. These pins transmit the serial bit stream for transmission. These signals interface directly with an isolation transformer.
2	TX2-	
3	RX2+	Analog Twisted Pair Ethernet Receive Differential Pair. These pins receive the serial bit stream from the isolation transformer.
6	RX2-	
4, 5, 7, 8	CT GND	Center Tap Ground – Center taps tied to ground through 75 ohm resistor and 1 nF capacitor.
9	ACT	Link/Activity signal indicates a Link is established or Activity is occurring
11	SPEED	Speed signal for 10BaseT or 100BaseT transfer rate
10, 12	+VCC	LED Power – The +3.3 volts for plus side of both LEDs.

Note: The shaded area denotes power or ground.

Audio Interface (J4)

The audio solution on the ReadyBoard 800 is provided by the (Southbridge) I/O Hub (82801DBM) and the on-board Audio CODEC (ALC202A). These two chips use a digital interface to communicate between the two, which is defined by AC'97 and is revision 2.3 compliant. The input or output signals for the audio interface go through the 16-pin connector (J4) to an external cable and/or board, which has the respective audio connections. The PC Beep Speaker signal from the I/O Hub is also fed to the on board Audio CODEC to provide a PC Beep signal for the stereo line out connections.

Audio CODEC (ALC202A) features

- AC'97 Rev 2.3 compliant
- 18-bit full duplex performance
- Variable sampling rate at 1 Hz resolution
- Stereo (Left and Right) Line In
- Stereo (Left and Right) Line Out
- Microphone (mono) in
- PC "Beep" speaker signal is also fed to the CODEC for the Line Out (Left and Right) channels

Table 3-15 describes the Audio interface (J4) pin/signals on 16-pins, 2 rows, odd/even (1, 2) with 2 mm pin spacing.

Table 3-15. Audio Interface Pin/Signal Descriptions (J4)

Pin #	Signal	Description
1, 3	NC	Not Connected
2, 4, 7, 8, 11, 12, 13, 14, 16	GND_AUD	Audio ground
5	LINE_OUTL	Line Out signal left channel
6	LINE_OUTR	Line Out signal right channel
9	LINE_INL	Line in signal left channel
10	LINE_INR	Line in signal right channel
15	MICIN	Microphone signal in

Note: The shaded area denotes power or ground.

Video Interfaces (J14, J21)

The Graphics & Memory Hub (Northbridge) chip (82855GME) provides the graphics control and video signals to the traditional glass CRT monitors and the LVDS flat panel displays. The chip features are listed below:

- Supports 2D/3D graphics with extensive set of instructions including:
  - 3D rendering and display
  - BLT operations
  - MPEG2 decode acceleration
  - 3D overlay

CRT features:

- Provides an integrated 350 MHz, 24-bit RAMDAC to drive a progressive scan analog monitor and outputs to three 8-bit DACs provide the R, G, and B signals to the monitor.
- Supports resolutions up to 1600 x 1200 at 85 Hz refresh, or up to 2048x1536 at 75 Hz refresh
- Supports a maximum allowable video frame buffer size of 64 MB UMA (Unified Memory Architecture)
- Supports AGP 4X equivalent graphics performance

LVDS Flat Panel features:

- Supports an integrated dual channel LVDS flat panel interface
- Supports LVDS flat panel resolutions up to UXGA + (1600x1200)
- Supports a maximum pixel format of 18 bpp (with SSC supported frequency range from 25 MHz to 112 MHz (single channel/dual channel)
- Supports 1 or 2 channel LVDS outputs
- The 82855GME chip only supports the LVDS port on Pipe B of two pipelines
- Supports panel up-scaling (to fit a smaller source image onto a specific native panel size) as well as panning and centering

Table 3-16 describes the CRT pin/signals of a standard 15-pin video connector. Table 3-17 describes the LVDS pin/signals on 30-pins, 2 rows, odd/even (1, 2) with 2 mm pin spacing.

CRT Interface (J21)

Table 3-16. CRT Interface Pin/Signal Descriptions (J21)

Pin #	Signal	Description
1	RED	Red – This is the Red analog output signal to the CRT.
2	GREEN	Green – This is the Green analog output signal to the CRT.
3	BLUE	Blue – This is the Blue analog output signal to the CRT.
4	NC	Not connected
5	GND	Ground
6	GND	Ground
7	GND	Ground
8	GND	Ground
9	NC	Not connected
10	GND	Ground
11	NC	Not connected
12	DDCA	Display Data Channel Data – This signal line provides information to the CPU through the Graphics & Memory Hub about the monitor type, brand, and model. This is part of the Plug and Play standard developed by the VESA trade association.
13	HSYNC	Horizontal Sync – This signal is used for the digital horizontal synchronous output to the CRT.
14	VSYNC	Vertical Sync – This signal is used for the digital vertical synchronous output to the CRT.
15	DDCLK	Display Data Channel Clock – This signal provides the data clock to the CPU through the Graphics & Memory Hub from the monitor. This is part of the Plug and Play standard developed by the VESA trade association.

Note: The shaded area denotes power or ground.

LVDS Interface (J14)

Table 3-17. LVDS Interface Pin/Signal Descriptions (J14)

Pin #	Signal	Description	Line	Channel
1	+12V	+12 Volts		
2	VCC_LCD	+3.3 Volts or +5 Volts Depends on JP4 setting (+3.3V **Default**)		
3	GND	Ground	GND	
4	GND	Ground		
5	LVDSB_Clk+	Clock Positive Output	Clk	Channel 2
6	LVDSB_Clk-	Clock Negative Output		
7	LVDSB_Y3+	Data Positive Output	3	
8	LVDSB_Y3-	Data Negative Output		
9	LVDSB_Y2+	Data Positive Output	2	
10	LVDSB_Y2-	Data Negative Output		
11	LVDSB_Y1+	Data Positive Output	1	
12	LVDSB_Y1-	Data Negative Output		
13	LVDSB_Y0+	Data Positive Output	0	
14	LVDSB_Y0-	Data Negative Output		
15	LCD_BKLTCTL	LCD Backlight Control		
16	LCD_EN	LCD Enable		
17	LVDSA_Clk+	Data Positive Output	Clk	Channel 1
18	LVDSA_Clk	Data Negative Output		
19	LVDSA_Y3+	Data Positive Output	3	
20	LVDSA_Y3	Data Negative Output		
21	LVDSA_Y2+	Data Positive Output	2	
22	LVDSA_Y2	Data Negative Output		
23	LVDSA_Y1+	Data Positive Output	1	
24	LVDSA_Y1-	Data Negative Output		
25	LVDSA_Y0+	Data Positive Output	0	
26	LVDSA_Y0-	Data Negative Output		
27	LVDS_DDCPClk	LVDS Clock		
28	LVDS_DDCPData	LVDS Data		
29	LCD_BKLEN	LCD Backlight Enable		
30	NC	Not connected		

Note: The shaded area denotes power or ground.

NOTE Pins 17-26 constitute 1st channel interface of two channels, or a single channel interface.

Pins 5-14 constitute 2nd channel interface of two channels.

Miscellaneous

Utility Interface (J12)

- Power-On – This control signal is provided externally through a switch by connecting ground to pin-1 on the Utility connector (J12).
- Reset Switch – This signal is provided externally through a switch by connecting ground to pin-3 on the Utility connector (J12). This signal line is shared with Reset Switch (SW1).
- PC Beep Speaker – The output signals from the I/O Hub (82801DBM) and the Super I/O (W83627HF) are fed to pin-5 of the Utility connector (J12) through an OR circuit, and in conjunction with the +5V (pin-4), drives an external PC Beep speaker. The PC Beep speaker signal from the I/O Hub is also fed to the on-board Audio CODEC to provide a PC Beep signal for the Line out connections.

Table 3-18. Utility Interface Pin/Signal Descriptions (J12)

Pin #	Signal	Description
1	PS_On	Power On input (connect between pins 1 & 2)
2	GND	Ground
3	RST_SW	Reset Switch input or output (connect between pins 3 & 2)
4	+5V	+5 Volts
5	Speaker	PC Beep Speaker + Output (connect between pins 5 & 4)

Note: The shaded area denotes power or ground.

Reset Switch (J20)

The reset switch (SW1), located on the board edge, provides an internal reset signal (momentary ground) to the ReadyBoard 800. The reset switch (J20) shares the reset line with pin-3 of the Utility interface (J12).

Keyboard/Mouse Interface (J19)

The PS/2 Keyboard and Mouse signal lines share the same mini-DIN connector (J19). A PS/2 Y-cable is required for connection to the PS/2 connector (J19), on the board edge.

NOTE	The keyboard and mouse are not interchangeable on the Y-cable, since each device has a specific connector on the Y-cable. The Super I/O senses when each device is connected and provides the appropriate signals.

Table 3-19. Keyboard/Mouse Interface Pin/Signal Descriptions (J19)

Pin #	Signal	Description
1	KB_Data	Keyboard data
2	MS_Data	Mouse Data
3	GND	Ground
4	PS2V5	Keyboard/Mouse Power (+ 5V +/- 5%)
5	KB_Clk	Keyboard Clock
6	MS_Clk	Mouse Clock
7, 8, 9, 10	GND	Ground (Used for grounding the shield on the connector)

Note: The shaded area denotes power or ground.

User GPIO Signals (J8)

The ReadyBoard 800 provides eight GPIO pins for custom use and the signals are routed to the J8 connector. Ampro has provided sample applications showing how to use the GPIO pins in the Miscellaneous Source Code Examples subdirectory, under the ReadyBoard 800 Software menu on the ReadyBoard 800 Doc & SW CD-ROM, *(CD-ROM\Software\Misc\GPIO)*.

For more information about the GPIO pin operation, refer to the datasheet specifications or Programming Manual for the Super I/O (W83627HF) controller at:

http://www.winbond-usa.com/products/winbond_products/pdfs/PCIC/W83627HF_F_HG_Ga.pdf

Table 3-20 list the GPIO pin/signals on a 10-pin, 2 rows, odd/even (1, 2) with 2 mm pin spacing.

Table 3-20. User GPIO Signals Pin/Signal Descriptions (J8)

Pin #	Signal	Description
1	GND	Ground
2	VCC	+5 Volts DC +/ 5%
3	GPIO4	User defined
4	GPIO5	User defined
5	GPIO6	User defined
6	GPIO7	User defined
7	GPIO0	User defined
8	GPIO1	User defined
9	GPIO2	User defined
10	GPIO3	User defined

Note: The shaded area denotes power or ground.

Infrared (IrDA) Port (J9)

The Infrared Data Association (IrDA) signals pass through a two-way communications header for an external IrDA device using infrared as the transmission medium. There are two basic infrared implementations provided; the Hewlett-Packard Serial Infrared (HPSIR) and the Amplitude Shift Keyed Infrared (ASKIR) methods. HPSIR is a serial implementation of infrared developed by Hewlett-Packard. The IrDA (HPSIR and ASKIR) signals share the same header as the IrDA model select signals. These signals are operating system (OS) and/or application dependent and are based on the user's application, but can be configured and enabled in BIOS Setup Utility. .

The HPSIR method allows serial communication at baud rates up to 115k baud. Each word is sent serially beginning with a zero value start bit. A zero is sent when a single infrared pulse is sent at the beginning of the serial bit time. A one is sent when no infrared pulse is sent during the bit time.

The Amplitude Shift Keyed infrared (ASKIR) allows serial communication at baud rates up to 19.2 k baud. Each word is sent serially beginning with a zero value start bit. A zero is sent when a 500 kHz waveform is sent for the duration of the serial bit time. A one is sent when no transmission is sent during the serial bit time.

Both of these methods require an understanding of the timing diagrams provided in the Super I/O controller (W83627HF) specifications available from the manufacture's web site and referenced earlier in this manual. For more information, refer to the Winbond W83627HF specifications and the Infrared Data Association web site at http://www.irda.org.

NOTE	For faster speeds and infrared applications not covered in this brief description, refer to the W83627HF chip specifications by Winbond Electronics Corp.

Table 3-21. Infrared Interface Pin/Signal Descriptions (J9)

Pin #	Signal	Description
1	VCC	+5 Volts DC +/ 5%
2	IRTX	IR Transmit Data
3	CIRRX	IR Mode Select
4	IRRX	IR Receive Data
5	GND	Ground

Note: The shaded area denotes power or ground.

System Management Bus (SMBus, J25)

The I/O Hub (Southbridge) chip (82801DBM) contains both a host and slave SMBus port; but the host cannot access the slave internally. The slave port allows an external master access to the I/O Hub through connector (J25). The master contained in the I/O Hub (82801DBM) is used to communicate with the SODIMM EPROM, Super I/O, Ethernet 1 and 2, and the clock generator. Table 3-22 lists the device name and corresponding reserved binary addresses on the SMBus. Table 3-23 lists the SMBus pin/signals on 5-pins, 1 row, 2 mm pin spacing on the external SMBus connector (J25). .

Table 3-22. SMBus Reserved Addresses

Component	Address Binary
SODIMM EPROM	$1010{,}000x_b$
Clock Generator (ICS950201)	$1101{,}001x_b$
I/O Hub (82801DBM)	$1000{,}100x_b$
I/O Hub (82801DBM)	$0001{,}000x_b$

Note: The I/O Hub has two reserved addresses.

Table 3-23. SMBus Signals Pin/Signal Descriptions (J25)

Pin #	Signal	Description
1	VCC5Dual	+5V standby voltage
2	SMBCLK	SMBus Clock
3	SMBDATA	SMBus Data
4	SMBALERT*	SMBus Alert
5	GND	Ground

Notes: The shaded area denotes power or ground. The signals marked with * = Negative true logic.

Real Time Clock (RTC)

The I/O Hub contains a Real Time Clock (RTC) and an external Lithium Battery (B1) provides power for the RTC and the CMOS RAM through connector BT1. The CMOS RAM is backed up with a Lithium Battery. If the battery is not present or defective, the BIOS has a battery-free boot option to complete the boot process.

Oops! Jumper (BIOS Recovery)

The Oops! jumper is provided in the event the BIOS settings you've selected prevent the system from booting, but does not reset CMOS or change the Time & Date in the BIOS. Refer to the CMOS Normal/Clear jumper (JP2) to reset the BIOS and change the Time & Date.

By using the Oops! jumper, you can prevent the current BIOS settings in Flash from being loaded, forcing the use of the default BIOS settings. Connect the DTR pin to the RI pin on Serial port 1 (COM 1) prior to applying power to prevent the current BIOS settings from loading. After booting with the Oops! jumper in place, remove the Oops! jumper and go into BIOS Setup Utility. Change the desired BIOS settings, or select the default settings, and save the changes before rebooting the system.

To convert the Serial 1 interface to an Oops! jumper, short together the DTR (4) and RI (9) pins on the Serial Port 1 DB9 connector as shown in Figure 3-2.

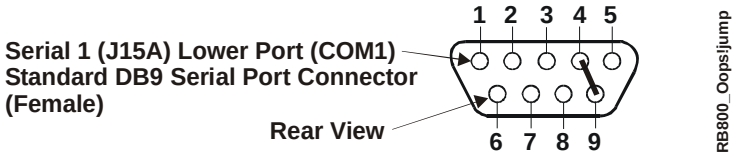


Figure 3-2. Oops! Jumper Connection

Temperature Monitoring

The Super I/O controller (W83627HF) performs the temperature monitoring function and has inputs directly from the only thermistor on the board and the thermal diode in the CPU. The thermistor (RT2) is located between the CPU and Super I/O chip on the underside of the board.

NOTE	The ReadyBoard 800 requires a heatsink for all processors, but no fan, except the 1.8 GHz Pentium CPU.

Remote Access (Serial Console)

The ReadyBoard 800 supports the Remote Access (serial console or console redirection) feature. The remote access (serial console) can be accessed by an ANSI-compatible serial terminal, or the equivalent terminal emulation software running on another system. This can be very useful when setting up the BIOS on a production line for systems that are not connected to a keyboard and display.

Serial Console Setup

The serial console feature is implemented by connecting a standard null modem cable or a modified serial cable (or "Hot Cable") between one of the serial ports, such as Serial 1 (J15A), and the serial terminal or a PC with communications software. The BIOS Setup Utility controls the serial console settings on the ReadyBoard 800. Refer to Chapter 4, BIOS Setup Utility to set the serial console option, using a serial terminal, or PC with communications software.

Hot (Serial) Cable

To convert a standard serial cable to a Hot Cable, certain pins must be shorted together at the Serial port connector or on the DB9 connector. For example, short the RTS (7) and RI (9) on the respective DB9 port connector as shown in Figure 3-3.

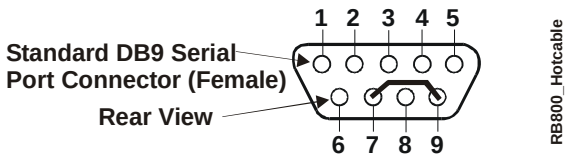


Figure 3-3. Hot Cable Jumper

Watchdog Timer (WDT)

The watchdog timer (WDT) restarts the system if an error or mishap occurs, allowing the system to recover from the mishap, even though the error condition may still exist. Possible problems include failure to boot properly, loss of control by the application software, failure of an interface device, unexpected conditions on the bus, or other hardware or software malfunctions.

The WDT (watchdog timer) can be used both during the boot process and during normal system operation.

- During the boot process – If the operating system fails to boot in the time interval set in the BIOS, the system will reset.

  Enable the WDT in the Advanced BIOS Features of BIOS Setup Utility. Set the WDT for a time-out interval in seconds, between 1 and 255, in one second increments. Ensure you allow enough time for the operating system (OS) to boot. The OS or application must tickle (reset) the WDT before the timer expires. This can be done by accessing the hardware directly or through a BIOS call.

- During System Operation – An application can set up the WDT hardware through a BIOS call, or by accessing the hardware directly. Some Ampro Board Support Packages provide an API to the WDT. The application must tickle (reset) the WDT before the timer expires or the system will be reset. The BIOS implements interrupt 15 function 0x0C3h to manipulate the WDT.

- Watchdog Code examples – Ampro has provided source code examples on the ReadyBoard 800 Doc & SW CD-ROM illustrating how to control the WDT. The code examples can be easily copied to your development environment to compile and test the examples, or make any desired changes before compiling. Refer to the WDT Readme file in the Miscellaneous Source Code Examples subdirectory, under the ReadyBoard 800 Software menu on the ReadyBoard 800 Doc & SW CD-ROM.

Power Interfaces (J1, J2)

The ReadyBoard 800 uses various voltages onboard, but only one voltage is required externally (+5 volts) through the external connector, which uses a 4-pin header with 0.200" (5.08 mm) spacing. The optional +12V volts is also provided on the input connector as a pass through voltage, but is not used on the board except for CPU Fan, LVDS power, PCI-104 bus, and optional ISA bus power. All other onboard voltages, including the CPU core voltages, are derived from the externally supplied +5 volts DC +/- 5%.

Power In Interface (J2)

Table 3-24 list the pin outs and signals for Power interface connector (J2).

Table 3-24. Power In Interface Pin/Signal Descriptions (J2)

Pin #	Signal	Description
1	+5V	+5.0 volts DC +/- 5%
2	GND	Ground
3	GND	Ground
4	+12V	This pass through +12 voltage is primarily for PCI-104 bus power, CPU fan, and LCD power (may also be backlight power).

Notes: The shaded area denotes power or ground. The +12V on the Power Interface connector (J2) is used for the LVDS (LCD panel), PCI-104 Bus, CPU Fan, and optional ISA Bus power, but may also be supplied externally.

Power-On Interface (J1)

The signals on this connector allow the ATX power supply to be turned off (soft off) from the ReadyBoard 800 by operating system (OS) control. If you use a non-ATX power supply (lab supply or AT power supply) you must connect J1 pin-1 to +5V (pin-1 on J2) to enable the ReadyBoard 800 to completely power on. However, if you use a non-ATX power supply, then you won't have the soft off feature for sleep states normally provided by ATX power supplies.

Table 3-25. Power-On Header Pin/Signal Descriptions (J1)

Pin #	Signal	Description
1	VCC5SBY	+5V Standby Voltage – This voltage (+5V, 100 mA minimum) is supplied from ATX power supply and is required for normal operation and sleep states.
2	GND	Ground
3	PS_ON*	Power Supply On – This signal is sent to the ATX power supply from the ReadyBoard 800 to turn On the ATX power supply. This signal can also be used to turn Off the ATX power supply or go into a suspended or standby state.

Notes: The shaded area denotes power or ground. The signals marked with * = Negative true logic.

NOTE	If the +5V suspend voltage is not present on the Power-On header (J1, pin-1) the ReadyBoard 800 will not completely power on. The board will have power (+5V) and Power On LED is lit (green), but it will never power up completely, because it can not start the boot process.

CPU Fan (J7)

Table 3-26 lists the pins and signals of the CPU Fan and it has 3 pins, single row, with 0.100" pin spacing.

Table 3-26. CPU Fan (J7)

Pin #	Signal	Description
1	Fan_Tach	Fan Tachometer – This signal indicates Fan speed.
2	+12V	+12.0 volts DC +/- 5%
3	GND	Ground

Note: The shaded area denotes power or ground.

NOTE	The ReadyBoard 800 provides the pass through +12 volts on the Power In (J2) connector to the CPU fan (J7) connector, the PCI-104 connector (J3), and the LVDS connector (J14).

CAUTION	To prevent damage to the 1.8 GHz CPU, you must supply +12 volts to the Power In connector (J2) for the fan voltage on the CPU Fan connector (J7). The +12 volt fan will only operate on the +12 pass through voltage provided by Power In connector (J2).

Power and Sleep States

The following information only applies if an ATX power supply is used to provide power to the ReadyBoard 800. If a non-ATX power supply is used, then the ReadyBoard 800 is only controlled by the Power On/Off switch on the power supply and the various sleep states are not available. The sleep states are OS dependent and not available if your OS does not support power management based on the ACPI standard.

Power On Switch

The Power On switch turns the ReadyBoard 800 and its attached power supply to a fully On condition, if you are using an ATX power supply. Normally, if the operating system (OS) supports sleep states, the OS will turn Off the ReadyBoard and its power supply during the OS shut down process. If the OS supports sleep states, the Power On button typically, will also transition the ReadyBoard and its power supply between a fully Powered On state, various sleep states depending on the OS control setting, and a fully Powered Off state. If the OS does not support sleep states, then the Power On button only turns power On or Off to the ReadyBoard 800.

An OS supporting ACPI, typically allows the Power-On switch to be configured through a user interface. The Power-On switch for the ReadyBoard 800 is provided externally by connecting a momentary switch between pins-1 and -2 on the Utility connector (J12). The power on signal occurs when ground is placed on pin-1 of J12.

Sleep States (ACPI)

The ReadyBoard 800 supports the ACPI (Advanced Configuration and Power Interface) standard, which is a key component of certain Operating Systems' (OS's) power management. The supported features (sleep states) listed here are only available when an ACPI-compliant OS is used for the operating system, such as Windows 2000/XP. The term "sleep" state refers to a low latency (reduced power consumption) state, which can be re-started (awakened) restoring full operation to the ReadyBoard 800.

If a computer is in one of the various sleep states, the computer appears to be off, indicated by such things as no display on the attached monitor and no activity for the connected floppy drive, CD-ROM, or hard drives. Normally, when a computer is in one of the various sleep states and it detects certain activity (i.e. power switch, mouse, keyboard, or certain types of LAN activity), it returns to a fully operational state.

NOTE	The ReadyBoard 800 supports various wake-up activities , including the Power-On switch to wake the ReadyBoard 800 from a powered down state, such as Standby (S1), Hibernate (S4) and Power Off (S5).

The ReadyBoard 800 supports four ACPI power states, depending on the operating system used and its ability to manage sleep states. Typically, the power on switch is used to wake up from a sleep state, or transition from one state to another, but this is dependent on the OS and the settings in BIOS Setup.

- 1st state is normal Power On (S0).
  - To go to a fully powered on state, the ReadyBoard 800 must either be powered Off (S5), or in a sleep state (S1 or S4), and then the Power-On switch is pressed for less than 4 seconds (default).
  - The ReadyBoard 800 can transition from this state (S0) to the various states described below, depending on the power management capability of the OS and how it is programmed.
- 2nd state is a standby state (S1).

  In this state there are very few internal operations taking placing, except for the internal RTC (real time clock), the Power On LED, and the contents of RAM. This includes no activity for the CPU, CD-ROM, or hard disk drives. The ReadyBoard 800 appears to be off except for the Power On LED.

- Normally, to enter this sleep state, the ReadyBoard 800 must be fully powered on (S0) and the OS transitions the ReadyBoard into this standby state (S1) under user control.
- To exit this sleep state, typically the Power-On switch is used to wake up the ReadyBoard 800 to restore full operation, including the Power On LED. Typically, pressing the Power-On switch for less than 4 seconds (default) will restore full operation.

- 3rd state is a hibernate or suspend-to-disk state (S4).

  In this state there are no internal operations taking placing, except for the Power On LED and the internal RTC. This includes no activity for the CPU, CD-ROM, or hard disk drives. The ReadyBoard 800 appears to be off, except for the Power On LED. Your system will take longer to wake-up from this sleep state, however, since your data is saved to the disk, it is more secure and should not be lost in the event of a power failure.

  - To enter a hibernate or suspend-to-disk state, the ReadyBoard 800 must be fully powered on and the OS transitions the ReadyBoard 800 into this sleep state (S4) under user control.
  - To exit this sleep state, typically pressing the Power-On switch for less than 4 seconds (default) will restore full operation.

- 4th state is the normal power Off or shutdown (S5).

  All activity stops except the Power On LED and the internal RTC clock, unless the power cord is removed from the AC power source.

  - To go to a fully powered down state, the ReadyBoard 800 must either be powered On, or in a sleep state, and then the Power-On switch is pressed for more than 4-to-6 seconds.
  - To go to a fully powered up state, press the Power-On switch for less than 4 seconds (default) and full operation is restored.

The OS may provide additional programming features to change the activation time for each state, and to shutdown or transition the ReadyBoard 800 at certain times, which depends on how the OS interface is programmed. Refer to the OS vender's documentation for power management under the ACPI standard.

NOTE	Some operating systems use the keyboard, mouse, Wake-on-Ring (serial port), and Wake-on-LAN (Ethernet port) as an activity to wake up the system from a sleep state. Refer to Table 3-27 for the conditions the ReadyBoard 800 currently supports for wake up activity.

Wake Up Activities

The wake up events listed in Table 3-27 can be used to wake up the ReadyBoard 800 from any of the states mentioned.

Table 3-27. Wake Up Activities and Conditions

Signal/Device	Condition
Power Switch	If the Power-On switch is pressed for more than 4-to-6 seconds, the system will wake up from any of the sleep states.
LAN Ports (2)	If Resume On LAN is [Enabled], then the system will wake from one of the sleep states through direct addressing, magic packets, or link status changes.
PS/2 Keyboard & Mouse	If you use a PS/2 keyboard or mouse, any activity from the keyboard or mouse could wake the system.
USB	If you use a USB keyboard or mouse instead of a PS/2 device, the USB device could wake the system.
Serial Ports (3)	If Resume On Ring is [Enabled], then three of the four Serial ports can wake the system.

Chapter 4 BIOS Setup Utility

Introduction

This chapter describes the BIOS Setup Utility menus and the various screens used for configuring the ReadyBoard 800. Some features in the Operating System or application software may require configuration in the BIOS Setup Utility screens.

This section assumes the user is familiar with general BIOS Setup Utility and does not attempt to describe the BIOS functions. Refer to the appropriate PC reference manuals for information about the onboard ROM-BIOS software interface. If Ampro has added to or modified the standard functions, these functions will be described.

The options provided for the ReadyBoard 800 are controlled by BIOS Setup Utility. BIOS Setup Utility is used to configure the board, modify the fields in the Setup screens, and save the results in the onboard configuration memory. Configuration memory consists of portions of the CMOS RAM in the battery-backed real-time clock chip and the flash memory.

The Setup information is retrieved from configuration memory when the board is powered up or when it is rebooted. Changes made to the Setup parameters, with the exception of the time and date settings, do not take effect until the board is rebooted.

Setup is located in the ROM BIOS and can be accessed while the board is in the Power-On Self Test (POST) state, just before starting the boot process. Typically, the screen displays a message indicating when you can press <Del> to enter the BIOS Setup Utility.

The BIOS Setup Utility is used to configure the ReadyBoard 800 using the following menus:

- Main
- Advanced
- PCIPnP
- Boot
- Security
- Chipset
- Power
- Exit

Table 4-1 summarizes the list of BIOS menus and some of the features available for ReadyBoard 800. The BIOS Setup Utility menu offers the menu choices listed above and the related topics and screens are described on the following pages.

Accessing BIOS Setup Utility (VGA Display)

To access the BIOS Setup Utility using a VGA display for the ReadyBoard 800:

1. Turn on the VGA monitor and the power supply to the ReadyBoard 800.
2. Start Setup by pressing the [Del] key, when the following message appears on the boot screen.

```
Press <Del> to run SETUP
```

NOTE	If the setting for *Quick Boot* is set to [Enabled], you may not see this prompt appear on screen if the monitor is too slow to display it on start up. If this happens, press the <Del> key early in the boot sequence to enter the BIOS Setup Utility.

3. Use the <Enter> key to select the screen menus listed in the Opening BIOS screen. See Figure 4-1.
4. Follow the instructions at the bottom of each screen to navigate through the selections and modify any settings.

Accessing BIOS Setup Utility (Remote Access)

Once you set up the BIOS Utility for Remote Access (serial console or console redirection) in VGA mode, entering the BIOS in the remote access mode, is very similar to the method used when entering the BIOS with a VGA display.

1. Turn on the power supply to the ReadyBoard 800 and access the BIOS Setup Utility in VGA mode.
2. Set the BIOS feature *Remote Access* to [Enabled] under the **Advanced** menu.
3. Accept the default options or make your own selections for the balance of the Remote Access fields and record your settings.
4. Ensure you select the type of remote serial terminal you will be using and record your selection.
5. Select *Save Changes and Exit* and then shut down the ReadyBoard 800.
6. Connect the remote serial terminal (or the PC with communications software) to the COM port you selected on the ReadyBoard 800 using a Hot Cable or a standard null-modem serial cable.
7. Turn on the remote serial terminal (or the PC with communications software) and set it to the settings you selected and recorded earlier in the BIOS Setup Utility.

   COM1, 115200, 8 bits, 1 stop bit, no parity, no flow control, and [Always] for *Redirection After BIOS POST* are the default settings for the ReadyBoard 800.
8. Restore power to the ReadyBoard 800 and look for the screen prompt shown below.

```
Press ^C to run SETUP
```

9. Press the CTRL–C keys to enter Setup early in the boot sequence if *Quick Boot* is set to [Enabled].

   If *Quick Boot* is set to [Enabled], you may never see the screen prompt.
10. Use the <Enter> key to select the screen menus listed in the Opening BIOS screen. See Figure 4-1.

NOTE	The serial console port is not hardware protected, and is not listed in the COM table within BIOS Setup Utility. Diagnostic software that probes hardware addresses may cause a loss or failure of the serial console functions.

Table 4-1. BIOS Setup Utility Menus

BIOS Setup Utility Menu	Item/Topic
Main Settings	Date and Time
Advanced Settings	CPU Configuration, IDE Configuration, Floppy Configuration, Super I/O Configuration, Hardware Health Configuration, ACPI Configuration, MPS Configuration, Smbios Configuration, Remote Access (Serial Console) Configuration, and USB Configuration
PCIPnP (PCI, Plug n' Play)	PCI settings, Plug & Play settings, Interrupt settings and DMA channel settings, Reserved memory
Boot	Boot Settings Configuration, Boot Device Priority, Hard Disk Drives, Removable Drives, CD/DVD Drives
Security	Setting or changing Supervisor/User Passwords, Boot Sector Virus Protection
Chipset	Northbridge Configuration, Southbridge Configuration
Power	Power Management (APM) and Resume Power conditions
Exit	Exiting with or without changing settings, Loading Optimal or Fail-safe conditions

BIOS Setup Utility Menus

Main Menu Screen

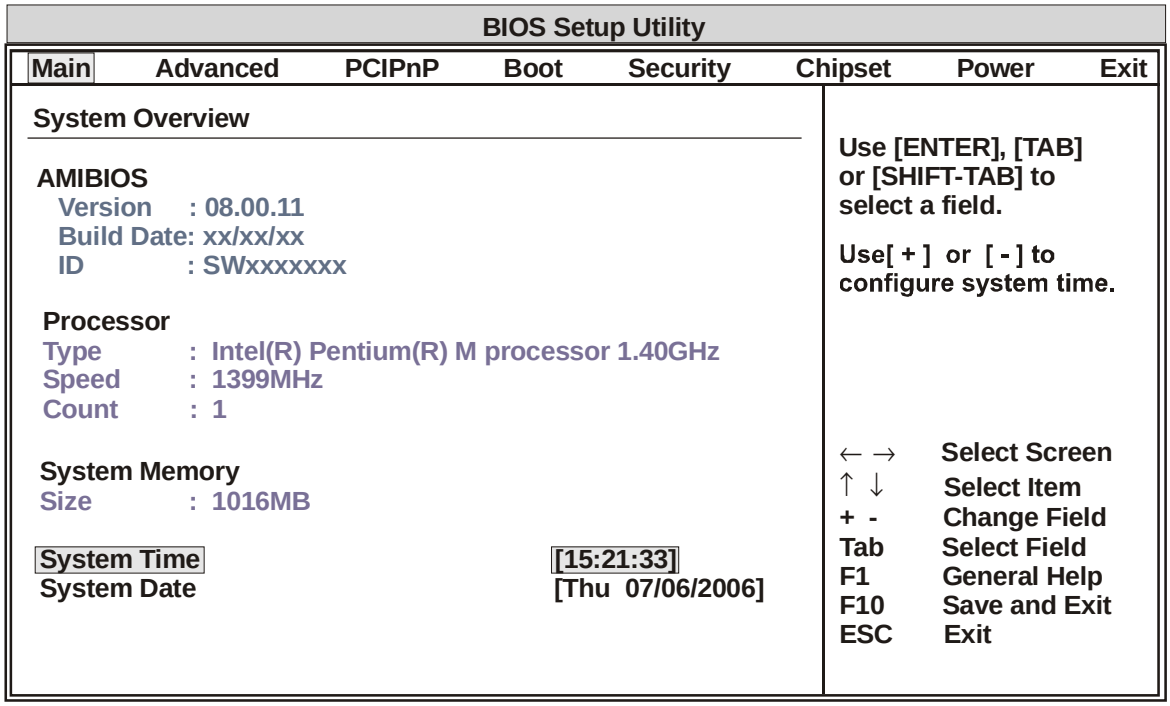


Figure 4-1. Main Menu Screen

- **Date & Time**
  - System Time (hh:mm:ss) – This is a 24-hour clock setting in hours, minutes, and seconds
  - System Date (day of week, mm:dd:yyyy) – This field requires the alpha-numeric entry of the day of week, calendar month, day of the month, and all 4 digits of the year, indicating the century plus year (*Thu 07/06/2006*).

NOTE	The Optimal Default values are shown highlighted as **bold text** and the Fail-safe Defaults are shown highlighted as *italic text* in the list of options. In many cases the Optimal values are the same as the Fail-safe values, so you will see text options as ***italic*** and ***bold*** text at the same time. Refer to the right of the BIOS screens for the navigation instructions when making selections.

Table 4-2. Exiting and Loading Default Keys

Key	Description
F7	Discard Changes without leaving BIOS Setup Utility
F8	Load failsafe default settings.
F9	Load optimal default settings.
F10	Save Changes and Exit BIOS Setup Utility

Advanced Menu Screen

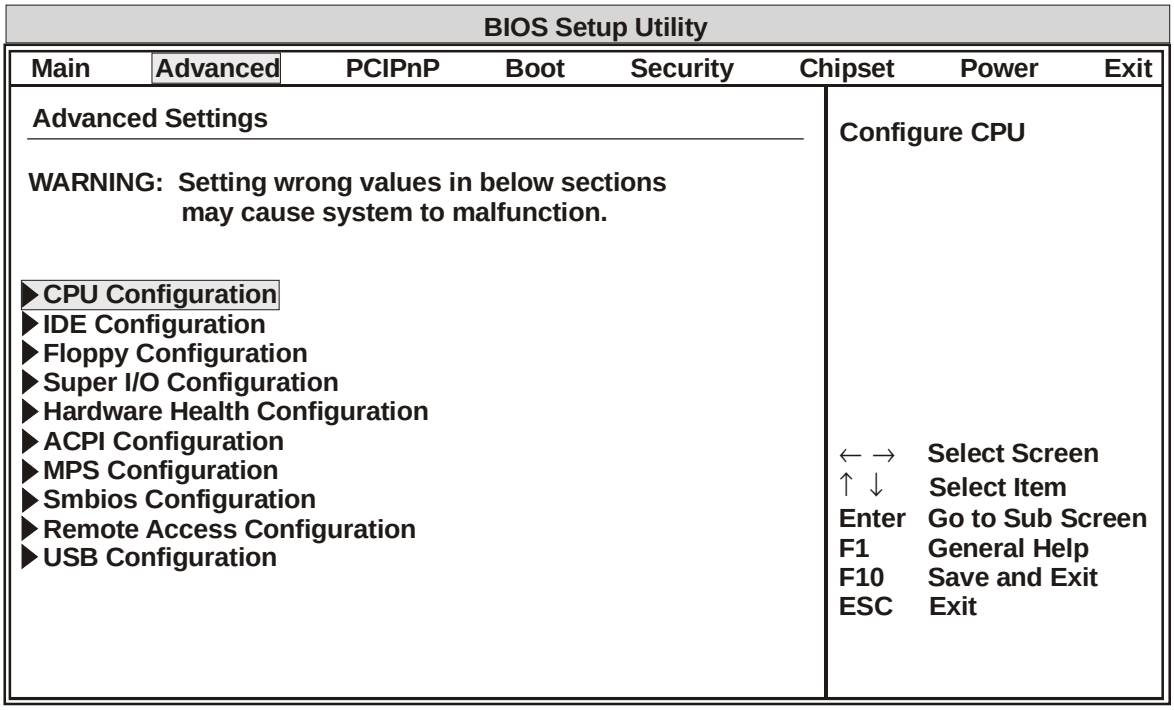


Figure 4-2. Advanced Menu Screen

Advanced Settings

>CPU Configuration

Configure advanced CPU settings

Module version - 11:05

Manufacture : Intel
Brand String : Intel® Pentium® M processor 1.40GHz
Frequency : 1.39GHz
FSB Speed : 400MHz

Cache L1 : 32kB
Cached L2 : 2048kB

- Execute Disable Bit – [Disabled] or [**Enabled**]

  This feature only appears for the CPUs that support it.

- Intel® SpeedStep(™) Technology – [***Maximum Speed***], [Minimum Speed], [Automatic], or [Disabled]

  This feature only appears for the Pentium CPUs that support it.

  Intel® Mobile Pentium® Processors with Intel® SpeedStep™ technology let you customize high performance computing on your embedded system. When powered by an AC outlet, the embedded system runs applications with speed virtually identical to a desktop system. When powered by a battery, the processor drops to a lower frequency (by changing the bus ratios) and voltage, conserving battery life while maintaining a high level of performance. Manual override lets you boost the frequency back to the high frequency when on battery, allowing you to customize performance.

>IDE Configuration

- OnBoard PCI IDE Controller – [Disabled], [Primary], [Secondary], or [***Both***]

  This item specifies the IDE channels used by the onboard PCI IDE controller.

  - If [Disabled] is selected, the ReadyBoard 800 is prevented from using either of the onboard IDE controllers.
  - If [Primary] is selected, the BIOS only detects the Primary IDE channel, including both Primary Master and Primary Slave.
  - If [Secondary] is selected, the BIOS only detects the Secondary IDE channel, including both Secondary Master and Secondary Slave.
  - If [Both] is selected, both Primary and Secondary IDE channels will be detected, including Master and Slave for each channel.

- OnBoard PCI IDE Operate Mode – [***Legacy Mode***] or [Native Mode]

  Native mode is only used with Windows XP.

  - Primary IDE Master – [Not Detected] or [Device type]
    - Type – [Not Installed], [***Auto***], [CD/DVD], or [ARMD]

      This field sets the type of device the BIOS attempts to boot from after the Power On Self Test (POST) has completed.

      * If [Not Installed] is selected, the BIOS is prevented from searching for an IDE disk drive on the specified channel.
      * If [Auto] is selected, the BIOS auto any detects IDE disk drives on the specified channel. This is the default setting and should be used if an IDE hard disk drive is attached to the specified IDE channel.
      * If [CD/DVD] is selected, the BIOS only searches for an IDE CD-ROM or IDE DVD device on the Primary IDE channel. The BIOS will not attempt to search for other types of IDE disk devices on the specified channel.
      * If [ARMD] is selected, the BIOS detects an ATAPI Removable Media Device on the specified IDE channel. This includes, but is not limited to ZIP drives and LS-120 drives.

    - LBA/Large Mode – [Disabled] or [***Auto***]

      This field sets the LBA (Logical Block Addressing) on the IDE disk drive. In LBA mode [***Auto***] the drive capacity can exceed 137 GB.

    - Block (Multi-Sector Transfer) – [Disabled] or [***Auto***]

      This field sets the block mode multi-sector transfers option and allows the BIOS to auto detect device support for Multi-Sector Transfers on the specified channel. Block mode boosts IDE drive performance by increasing the amount of data transferred. Only 512 bytes of data can be transferred per interrupt if block mode is not used. Block mode allows transfers of up to 64 kB per interrupt.

      * If [Auto] is selected, the BIOS will auto detect the number of sectors per block for transfer from the hard disk drive to the memory. The data transfer to and from the device will occur multiple sectors at a time.

    - PIO Mode – [***Auto***], [0], [1], [2], [3], or [4]

      This field sets the IDE PIO (Programmable I/O) mode and programs the timing cycles between the IDE drive and the programmable IDE controller. As the PIO mode increases, the cycle time decreases.

      * If [Auto] is selected, the BIOS auto detects the PIO mode.

- If [0] is selected, the BIOS uses PIO mode 0, with a data transfer rate of 3.3 MBs.
- If [1] is selected, the BIOS uses PIO mode 1, with a data transfer rate of 5.2 MBs.
- If [2] is selected, the BIOS uses PIO mode 2, with a data transfer rate of 8.3 MBs.
- If [3] is selected, the BIOS uses PIO mode 3, with a data transfer rate of 11.1 MBs.
- If [4] is selected, the BIOS uses PIO mode 4, with a data transfer rate of 16.6 MBs.

- DMA Mode – [***Auto***], [SWDMA0], [SWDMA01], [SWDMA2], [MWDMA0], [MWDMA1], [MWDMA2], [UDMA0], [UDMA1], or [UDMA2]

  This field allows you to select DMA modes and adjust the respective transfer rate. The list of DMA modes are dependent on the device's DMA characteristics.

  SWDMAn = Single Word DMA mode n

  MWDMAn = Muliti Word DMA mode n

  UDMAn = Ultra DMA mode n

  - If [Auto] is selected, the BIOS auto detects the DMA Mode. Use this value if the IDE disk drive support cannot be determined.
  - If [SWDMA0] is selected, the BIOS uses Single Word DMA mode 0, with a data transfer rate of 2.1 MBs.
  - If [SWDMA1] is selected, the BIOS uses Single Word DMA mode 1, with a data transfer rate of 4.2 MBs.
  - If [SWDMA2] is selected, the BIOS uses Single Word DMA mode 2, with a data transfer rate of 8.3 MBs.
  - If [MWDMA0] is selected, the BIOS uses Muliti Word DMA mode 0, with a data transfer rate of 4.2 MBs.
  - If [MWDMA1] is selected, the BIOS uses Muliti Word DMA mode 1, with a data transfer rate of 13.3 MBs.
  - If [MWDMA2] is selected, the BIOS uses Muliti Word DMA mode 2, with a data transfer rate of 16.6 MBs.
  - If [UDMA0] is selected, the BIOS uses Ultra DMA mode 0, with a data transfer rate of 16.6 MBs.
  - If [UDMA1] is selected, the BIOS uses Ultra DMA mode 1, with a data transfer rate of 25 MBs.
  - If [UDMA2] is selected, the BIOS uses Ultra DMA mode 2, with a data transfer rate of 33.3 MBs.

- S.M.A.R.T. – [***Auto***], [Disabled], or [Enabled]

  The Self-Monitoring Analysis and Reporting Technology (SMART) feature can help predict impending hard disk drive failures.

  - If [Auto] is selected, the BIOS auto detects hard disk drive support. Use this setting if the IDE disk drive support cannot be determined.
  - If [Disabled] is selected, the BIOS is prevented from using SMART feature.
  - If [Enabled] is selected, the BIOS uses the SMART feature on the hard disk, drives.

- 32Bit Data Transfer – [*Disabled*] or [**Enabled**]

  This field sets the 32-bit data transfer rate.

  If [Enabled] is selected, the BIOS uses 32-bit data transfers on the supported hard disk drive.

- Primary IDE Slave – [Not Detected] or [Device type]

  The descriptions used for the Primary IDE Master are the same for the Primary IDE Slave except where noted.

  - Type – [Not Installed], [***Auto***], [CD/DVD], or [ARMD]
  - LBA/Large Mode – [Disabled] or [***Auto***]
  - Block (Multi-Sector Transfer) – [Disabled] or [***Auto***]
  - PIO Mode – [***Auto***], [0], [1], [2], [3], or [4]
  - DMA Mode – [***Auto***], [SWDMA0], [SWDMA01], [SWDMA2], [MWDMA0], [MWDMA1], [MWDMA2], [UDMA0], [UDMA1], or [UDMA2]
  - S.M.A.R.T. – [***Auto***], [Disabled], or [Enabled]
  - 32Bit Data Transfer – [*Disabled*] or [**Enabled**]

- Secondary IDE Master – [**Not Detected**] or [Device type]

  The descriptions used for the Primary IDE Master are the same for the Secondary IDE Master except where noted.

  - Type – [Not Installed], [***Auto***], [CD/DVD], or [ARMD]
  - LBA/Large Mode – [Disabled] or [***Auto***]
  - Block (Multi-Sector Transfer) – [Disabled] or [***Auto***]
  - PIO Mode – [***Auto***], [0], [1], [2], [3], or [4]
  - DMA Mode – [***Auto***], [SWDMA0], [SWDMA01], [SWDMA2], [MWDMA0], [MWDMA1], [MWDMA2], [UDMA0], [UDMA1], or [UDMA2]
  - S.M.A.R.T. – [***Auto***], [Disabled], or [Enabled]
  - 32Bit Data Transfer – [*Disabled*] or [**Enabled**]

- Secondary IDE Slave – [**Not Detected**] or [Device type]

  The descriptions used for the Primary IDE Master are the same for the Secondary IDE Slave except where noted.

  - Type – [Not Installed], [***Auto***], [CD/DVD], or [ARMD]
  - LBA/Large Mode – [Disabled] or [***Auto***]
  - Block (Multi-Sector Transfer) – [Disabled] or [***Auto***]
  - PIO Mode – [***Auto***], [0], [1], [2], [3], or [4]
  - DMA Mode – [***Auto***], [SWDMA0], [SWDMA01], [SWDMA2], [MWDMA0], [MWDMA1], [MWDMA2], [UDMA0], [UDMA1], or [UDMA2]
  - S.M.A.R.T. – [***Auto***], [Disabled], or [Enabled]
  - 32Bit Data Transfer – [*Disabled*] or [**Enabled**]

- Hard Disk drive Write Protect – [***Disabled***] or [Enabled]

  This field protects the hard disk drive from being overwritten.

  * If [Disabled] is selected, the HDD operates normally, allowing Read, Write, and Erase functions to be performed on the IDE hard disk drive.
  * If [Enabled] is selected, the BIOS is prevents the IDE HDD from being erased.

- IDE Detect Time Out (Seconds) – [0], [5], [10], [15], [20], [25], [30], or [***35***]

  The field determines how long the BIOS searches for the available IDE devices on the specified channels. Some IDE HDDs take the BIOS longer to locate than others, but this field allows you fine-tune the settings to allow for faster boot times.

  * If [0] is selected, the BIOS does not search for an IDE device. This is the best setting to use if the onboard IDE controllers are set to a specific IDE HDD in the BIOS.
  * If [5] is selected, the BIOS stops searching for an IDE device after 5 seconds. A large majority of ultra ATA HDDs can be detected with within 5 seconds.
  * If [10] is selected, the BIOS stops searching for an IDE device after 10 seconds.
  * If [15] is selected, the BIOS stops searching for an IDE device after 15 seconds.
  * If [20] is selected, the BIOS stops searching for an IDE device after 20 seconds.
  * If [25] is selected, the BIOS stops searching for an IDE device after 25 seconds.
  * If [30] is selected, the BIOS stops searching for an IDE device after 30 seconds.
  * If [35] is selected, the BIOS stops searching for an IDE device after 35 seconds. This is the default setting and is the recommended setting when all IDE connectors are set to Auto.

- ATA (PI) 80 pin Cable Detection – [***Host & Device***], [Host], or [Device]

  This field selects the method used to detect the ATA (PI) 80-pin cable. The default setting for this field is 40-pin cable.

  * If [Host & Device] is selected, the BIOS uses both the onboard IDE controller and the IDE hard disk drive (HDD) to detect the type of IDE cable used.
  * If [Host] is selected, the BIOS uses only the onboard IDE controller to detect the type of IDE cable used.
  * If [Device] is selected, the BIOS uses only the IDE hard disk drive (HDD) to detect the type of IDE cable used.

NOTE	An 80-conductor ATA cable is required when operating with Ultra ATA/66, Ultra ATA/100 and Ultra ATA/133 IDE hard disk drives. The standard 40-conductor ATA cable cannot handle the higher speeds. Due to the plug compatibility of the 80-conductor ATA cable to the standard 40-conductor ATA cable, the BIOS must have a feature to set this or determine if the 80-conductor ATA cable is present. The BIOS detects a break in one of the lines on the 80-conductor ATA cable that is normally an unbroken connection in the standard 40-conductor ATA cable. If a faster speed is set in the BIOS than the connected cable can support, the BIOS instructs the IDE HDD to run at the correct speed for the cable type detected.

>Floppy Configuration

- Drive A – [Disabled], [360 kB, 5 1/4 "], [1.2 MB, 5 1/4"], [720 kB, 3 1/2"], [***1.44 MB, 3 1/2"],*** or [2.88 MB, 3.5"]
- Drive B – [***Disabled***], [360 kB, 5 1/4"], [1.2 MB, 5 1/4"], [720 kB, 3 1/2"], [1.44 MB, 3 1/2"], or [2.88 MB, 3.5"]

>Super I/O Configuration

- Onboard Floppy Controller – [Disabled] or [***Enabled***]
- Serial Port 1 Address – [Disabled], [***3F8/IRQ4***], [2F8/IRQ3], [3E8/IRQ4], or [2E8/IRQ3]
- Serial Port 2 Address – [Disabled], [3F8/IRQ4], [***2F8/IRQ3***], [3E8/IRQ4], or [2E8/IRQ3]
  - Serial Port 2 Mode – [***Normal***], [IrDA], or [ASK IR]
    - If [IrDA] or [ASK IR] are selected, the following items appear on screen.
      - IR I/O Pin select – [***SINB/SOUTB***] or [IRRX/IRTX]
      - IR Duplex mode – [***Half Duplex***] or [Full Duplex]
- Parallel Port Address – [***Disabled***], [378], [278], or [3BC]

  If [378], [278], or [3BC] are selected, the following items appear on screen.
  - Parallel Port Mode – [***Normal***], [Bi-Directional], [ECP], [EPP], or [ECP + EPP]
    - If [Normal] is selected, the standard parallel port mode is used. This is the default setting.
    - If [Bi-Directional] is selected, the data is sent to and received from the parallel port.
    - If [ECP] is selected, the following options are listed. The parallel port can be used with devices adhering to the Extended Capabilities Port (ECP) specification. ECP uses the DMA protocol to achieve data transfer rates up to 2.5 Megabits per second. ECP also provides symmetric bi-directional communication.
      - ECP Mode DMA Channel – [DMA0], [DMA1], or [***DMA3***]
    - If [EPP] is selected, the following options are listed. The parallel port can be used with devices adhering to the Enhanced Parallel Port (EPP) specification. EPP uses the existing parallel port signals to provide asymmetric bi-directional data transfer driven by the host device.
      - EPP version – [***1.9***] or [1.7]
    - If [ECP + EPP] is selected, the options for both are listed, with EPP options listed first.
  - Parallel Port IRQ – [IRQ5] or [***IRQ 7***]
- OnBoard CIR Port – [***Disabled***], [3E0], or [2E0]
  - CIR Port IRQ – [IRQ3], [IRQ4], [***IRQ10***], or [IRQ 11]
- Serial Port 3 – [Disabled], [3F8], [2F8], [***3E8***], [2E8], [2F0], or [2E0]
  - Serial Port 3 IRQ – [IRQ4], [IRQ9], [IRQ10], or [***IRQ 11***]
  - Select Serial Port 3 Type – [***RS232***] or [RS485]
- Serial Port 4 – [Disabled], [3F8], [2F8], [3E8], [***2E8***], [2F0], or [2E0]
  - Serial Port 4 IRQ – [IRQ3], [IRQ9], [***IRQ10***], or [IRQ 11]
  - Select Serial Port 4 Type – [*RS232*] or [RS485]

>Hardware Health Configuration

- H/W Health Function – [Disabled] or [**Enabled**]

  Hardware Health Event Monitoring

  - System Temperature [Current board temperature in °C/°F]
  - CPU Temperature [Current CPU die temperature in °C/°F]
  - VcoreA [Current CPU Core A reading]
  - VcoreB [Current CPU Core B reading]
  - +3.3Vin [Current +3.3 voltage reading]
  - +5Vin [Current +5 voltage reading]
  - +12Vin [Current +12 voltage reading]
  - -12Vin [Invalid voltage readings]
  - -5Vin [Invalid voltage readings]
  - +5VSBin [Current +5 standby voltage reading]

>ACPI Configuration

- Advanced ACPI Configuration
  - ACPI 2.0 Features – [No] or [***Yes***]
    - If [Yes] is selected, the BIOS will support the ACPI 2.0 specifications.
  - Headless Mode – [***Disabled***] or [Enabled]
    - If [Enabled] is selected, the ACPI FSDT (Fixed System Description Table) is updated to indicate headless operation mode through ACPI. Today, headless operation implies no keyboard or mouse.
- Chipset ACPI Configuration
  - APIC ACPI SCI IRQ – [***Disabled***] or [Enabled]

>MPS Configuration

- MPS Revision – [1.1] or [***1.4***]

>Smbios Configuration

- Smbios Smi Support – [Disabled] or [***Enabled***]

>Remote Access Configuration

- Remote Access – [***Hotcable***] or [Enabled]

  This field enables the Remote Access (Serial Console or Console Redirection) features.
  - Serial Port Number – [**COM1**] or [COM2]

    Base Address, IRQ [3F8h, 4]
  - Serial Port Mode – [***115200, 8, n, 1***], [57600, 8, n, 1], [38400, 8, n, 1], [19200, 8, n, 1], or [09600, 8, n, 1]
    - If [57600, 8, n, 1] is selected, the remote access operates at 57.6 kHz baud rate and there are 8 start bits, no parity, and 1 stop bit used.
  - Flow Control – [***None***], [Hardware], or [Software]
    - If [Hardware] is selected, flow control is handled by hardware.
    - If [Software] is selected, flow control is handled by software.

- Redirection After BIOS POST – [Disabled], [Boot Loader], or [***Always***]
- Terminal Type – [***ANSI***], [VT100], or [VT-UTF8]
  - If [VT-UTF8] is selected, the following item disappears from the screen.
    - VT-UTF8 Combo Key Support – [Disabled] or [***Enabled***]
- Sredir Memory Display Delay – [***No Delay***], [Delay 1 sec], [Delay 2 sec] or [Delay 4 sec]
  - If [Delay 4 sec] is selected,

>USB Configuration

Depending on the USB devices detected, examples similar to those listed below may be displayed.

Module Version - x.xx.xx-xx.x Or Module Version - x.xx.xx-xx.x

USB Devices Enabled: 2 drives

USB Devices Enabled: None:

- USB Function – [Disabled], [2 USB ports], or [***4 USB ports***]
- Legacy USB Support – [Disabled], [***Enabled***], or [Auto]

  This field supports the USB mouse and USB keyboard when no USB drivers are loaded for the operating system (OS). If this option is not enabled, the attached USB mouse and USB keyboard will not be available until a USB compatible OS is fully booted with all the USB drivers loaded.

NOTE	If this field is not enabled with [Enabled] or [Auto] the USB mouse and USB keyboard will not be recognized by the BIOS until the OS is fully booted and the USB drivers are loaded.

  - If [Enabled] is selected, USB devices may be used during boot time and while using DOS.
  - If [Auto] is selected, USB devices like, a USB keyboard or USB mouse will be automatically detected and if found, will be initialized and utilized during Boot time.
- USB 2.0 Controller – [**Enabled**] or [*Disabled*]
  - If [Disabled] is selected, the following item disappears from the screen.
    - USB 2.0 Controller Mode – [*Full Speed*] or [**Hi Speed**]

      This field configures the USB 2.0 controller for [Full Speed = 12 Mbps] or [Hi Speed = 480 Mbps]
- BIOS EHCI Hand-Off – [Disabled] or [***Enabled***]

  This field is used as work around for operating systems (OSs) that do not have EHCI hand-off support. The EHCI ownership change should be claimed by the EHCI driver.

>USB MASS Storage Device Configuration

- USB Mass Storage Reset Delay – [10 sec], [**20 sec**], [30 sec], or [40 sec]

  This field determines the number of seconds POST waits for the storage device after the start unit command is sent.
  - Device #1 – [Mfg + model or device type]
  - Emulation Type – [**Auto**], [Floppy], [Forced FDD], [Hard Disk], or [CDROM]

    This field emulates USB device types.
    - If this field is set to [Auto] it will emulate USB devices less than 530 MB as Floppy and devices larger than 530 MB as Hard Drives.
    - If the [Forced FDD] options is selected, a HDD formatted drive can be forced to boot as FDD (except ZIP drives).

The remaining fields only appear if the BIOS detects additional USB mass storage devices up to three more USB devices.

- Device #2 – [Mfg + model or USB device type]
- Emulation Type – [**Auto**], [Floppy], [Forced FDD], [Hard Disk], or [CDROM]
- Device #3 – [Mfg + model or USB device type]
- Emulation Type – [**Auto**], [Floppy], [Forced FDD], [Hard Disk], or [CDROM]
- Device #4 – [Mfg + model or USB device type]
- Emulation Type – [**Auto**], [Floppy], [Forced FDD], [Hard Disk], or [CDROM]

PCIPnP Menu Screen

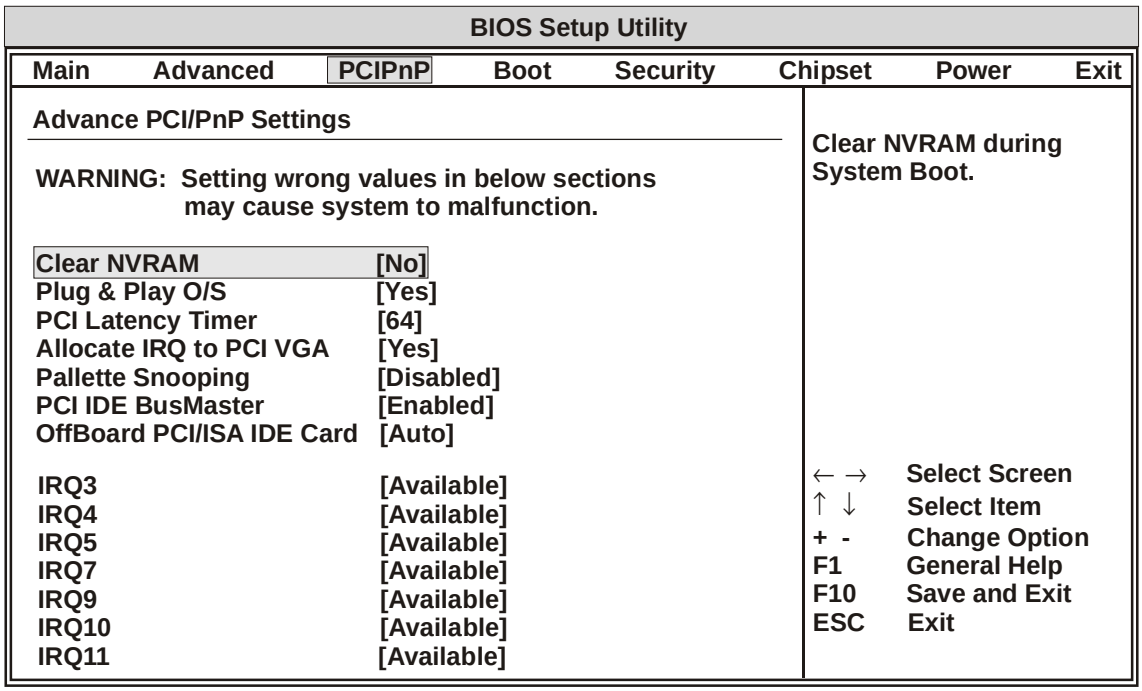


Figure 4-3. PCIPnP Menu Screen

Advanced PCI/PnP Settings

- Clear NVRAM – [***No***] or [Yes]

  This field is used to clear NVRAM during system boot.

- Plug & Play O/S – [No] or [***Yes***]

  * If [No] is selected, the BIOS is allowed to configure all the devices in the system.
  * If [Yes] is selected, the Operating System (OS) is allowed to change the interrupt, I/O, and DMA settings for the devices in the system. This is only used by Plug & Play capable OSs.

- PCI Latency timer – [32], [***64***], [96], [128], [160], [192], [224], or [248]

  This feature sets the latency of all PCI devices on the PCI bus. The various settings allow the PCI Latency timer to be adjusted to the number of clock cycles specified. The default setting [64] adjust the PCI Latency timer to 64 PCI clock cycles.

- Allocate IRQ to PCI VGA – [***Yes***] or [No]

  This field allows or restricts the system from giving the VGA adapter card an interrupt address.

  * If [Yes] is selected, the BIOS is allowed to allocate an IRQ to any VGA adapter card that uses the PCI local bus.

- Palette Snooping – [***Disabled***] or [Enabled]

  * If [Disabled] is selected, the BIOS prevents the VGA card from using Palette Snooping. This should not be changed unless the VGA card manufacturer requires this feature to be Enabled.

- PCI IDE BusMaster – [Disabled] or [***Enabled***]
  - If [Enabled] is selected, the BIOS allows the IDE controller on the PCI local bus to have bus mastering capabilities.
- OffBoard PCI/ISA IDE card – [***Auto***], [PCI Slot 1], [PCI Slot 2], [PCI Slot 3], or [PCI Slot 4]
  - If [Auto] is selected, BIOS is allowed to automatically select the location of an OffBoard PCI IDE adapter card. Don't select the other PCI slot positions, unless the IDE adapter card is installed in the respective card slot position. This is the default selection.
- IRQ3 – [***Available***] or [Reserved]
  - If [Available] is selected, the BIOS can assign this IRQ to a PCI/PnP device.
  - If [Reserved] is selected, the BIOS holds this IRQ for a legacy ISA device.
- IRQ4 – [***Available***] or [Reserved]
  - If [Available] is selected, the BIOS can assign this IRQ to a PCI/PnP device.
  - If [Reserved] is selected, the BIOS holds this IRQ for a legacy ISA device.
- IRQ5 – [***Available***] or [Reserved]
  - If [Available] is selected, the BIOS can assign this IRQ to a PCI/PnP device.
  - If [Reserved] is selected, the BIOS holds this IRQ for a legacy ISA device.
- IRQ7 – [***Available***] or [Reserved]
  - If [Available] is selected, the BIOS can assign this IRQ to a PCI/PnP device.
  - If [Reserved] is selected, the BIOS holds this IRQ for a legacy ISA device.
- IRQ9 – [***Available***] or [Reserved]
  - If [Available] is selected, the BIOS can assign this IRQ to a PCI/PnP device.
  - If [Reserved] is selected, the BIOS holds this IRQ for a legacy ISA device.
- IRQ10 – [***Available***] or [Reserved]
  - If [Available] is selected, the BIOS can assign this IRQ to a PCI/PnP device.
  - If [Reserved] is selected, the BIOS holds this IRQ for a legacy ISA device.
- IRQ11 – [***Available***] or [Reserved]
  - If [Available] is selected, the BIOS can assign this IRQ to a PCI/PnP device.
  - If [Reserved] is selected, the BIOS holds this IRQ for a legacy ISA device.
- IRQ14 – [***Available***] or [Reserved]
  - If [Available] is selected, the BIOS can assign this IRQ to a PCI/PnP device.
  - If [Reserved] is selected, the BIOS holds this IRQ for a legacy ISA device.
- IRQ15 – [***Available***] or [Reserved]
  - If [Available] is selected, the BIOS can assign this IRQ to a PCI/PnP device.
  - If [Reserved] is selected, the BIOS holds this IRQ for a legacy ISA device.
- DMA Channel 0 – [***Available***] or [Reserved]
  - If [Available] is selected, the BIOS can assign this DMA Channel to a PCI/PnP device.
  - If [Reserved] is selected, the BIOS holds this DMA Channel for a legacy ISA device.

- DMA Channel 1 – [***Available***] or [Reserved]
  - If [Available] is selected, the BIOS can assign this DMA Channel to a PCI/PnP device.
  - If [Reserved] is selected, the BIOS holds this DMA Channel for a legacy ISA device.
- DMA Channel 3 – [***Available***] or [Reserved]
  - If [Available] is selected, the BIOS can assign this DMA Channel to a PCI/PnP device.
  - If [Reserved] is selected, the BIOS holds this DMA Channel for a legacy ISA device.
- DMA Channel 5 – [***Available***] or [Reserved]
  - If [Available] is selected, the BIOS can assign this DMA Channel to a PCI/PnP device.
  - If [Reserved] is selected, the BIOS holds this DMA Channel for a legacy ISA device.
- DMA Channel 6 – [***Available***] or [Reserved]
  - If [Available] is selected, the BIOS can assign this DMA Channel to a PCI/PnP device.
  - If [Reserved] is selected, the BIOS holds this DMA Channel for a legacy ISA device.
- DMA Channel 7 – [***Available***] or [Reserved]
  - If [Available] is selected, the BIOS can assign this DMA Channel to a PCI/PnP device.
  - If [Reserved] is selected, the BIOS holds this DMA Channel for a legacy ISA device.
- Reserved Memory – [***Disabled***], [16k], [32k], or [64k]
  - If [Disabled] is selected, the BIOS is prevented from reserving memory for ISA devices.
  - If [64k] is selected, the BIOS reserves 64k of system memory for ISA devices.
- PCI Slot 1 – IRQ Preference– [***Auto***], [3], [4], [5], [7], [9], [10], [11], [12], [14], or [15]

  These fields select the PCI slot IRQ preference.
- PCI Slot 2 – IRQ Preference– [***Auto***], [3], [4], [5], [7], [9], [10], [11], [12], [14], or [15]
- PCI Slot 3 – IRQ Preference– [***Auto***], [3], [4], [5], [7], [9], [10], [11], [12], [14], or [15]
- PCI Slot 4 – IRQ Preference– [***Auto***], [3], [4], [5], [7], [9], [10], [11], [12], [14], or [15]

NOTE	Manually selecting IRQs for the PCI slots does not guarantee the PCI slot device will be configured with the selection. Typically, Plug & Play ISA cards (if present) are assigned the available resources before PCI devices.

Boot Menu Screen

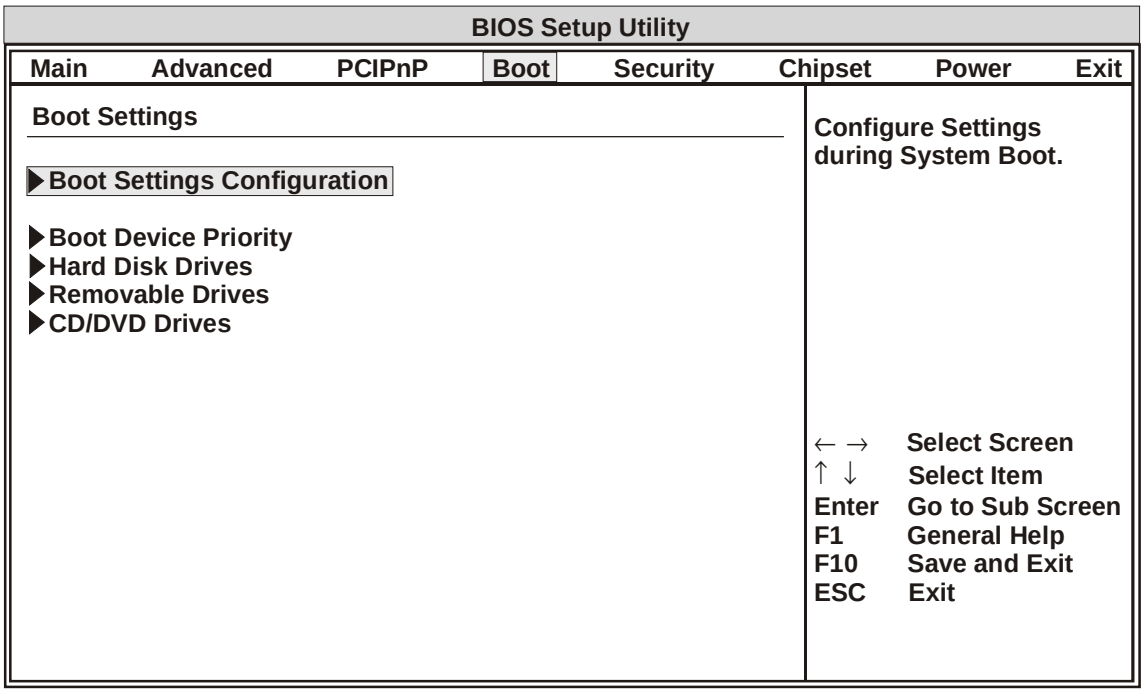


Figure 4-4. Boot Menu Screen

Boot Settings

The device categories appearing in the Boot screen (Hard Disk Drives, Removable Drives, and CD/DVD Drives) are dependent on the device types connected to the ReadyBoard 800 assemlby.

>**Boot Settings Configuration**

- Quick Boot – [Disabled] or [***Enabled***]
  - If [Disabled] is selected, the BIOS is allowed to perform all POST test, but this slows the boot process.
  - If [Enabled] is selected, the BIOS is allowed to skip certain POST tests to boot faster.
- Quiet Boot – [***Disabled***] or [Enabled]
  - If [Disabled] is selected, the BIOS is allowed to display the POST messages on screen.
  - If [Enabled] is selected, the BIOS displays the customized splash screen (OEM boot logo) on screen. The splash screen image (or boot logo) will appear on the display instead of the POST messages.

    For more information about how to customize a splash screen image(OEM boot logo), refer to the Splash Screen files on the ReadyBoard 800 Doc & SW CD-ROM in the *CD-ROM/Software/Misc/Splash* directory for instructions on creating your own logo to display.
- AddOn ROM Display Mode – [***Force BIOS***] or [Keep Current]
  - If [Force BIOS] is selected, any third party BIOS or add-on ROM messages will be displayed on screen during the boot process.
  - If [Keep Current] is selected, no third party BIOS messages will be displayed on screen during the boot process.

- Bootup Num-Lock – [***Off***] or [On]

  This field enables or disables the Num-Lock (Number Lock) keypad, including the 10-key numeric keys, to be turned on or off automatically when the system boots up. The field selection will remain unchanged until the Num-Lock key on the keyboard is pressed to change the Num-Lock state. .

- PS/2 Mouse Support – [Disabled], [Enabled], or [***Auto***]
  - If [Disabled] is selected, the PS/2 Mouse will not have access to system resources and will not be active after boot up.
  - If [Enabled] is selected, the PS/2 Mouse can be used and will have access to system resources after boot up.
  - If [Auto] is selected, the BIOS will detect the PS/2 Mouse automatically, if present, during the boot process. The PS/2 Mouse will have access to system resources and be active after boot up.

- Wait for 'F1' If Error – [***Disabled***] or [Enabled]
  - If [Disabled] is selected, this does not allow for user intervention if an error occurs. Use this setting only when a known BIOS error will appear.
  - If [Enabled] is selected, allows the BIOS to display an Error message indicating when an error has occurred during POST (power on self test) and wait for you to respond by hitting the <F1> key. Pressing <F1> will enter Setup and the BIOS setting can be adjusted to fix the problem.

- Hit 'Del' Message Display – [Disabled] or [***Enabled***]
  - If [Disabled] is selected, the BIOS will not place the "Press 'DEL' to enter Setup" message on screen during the boot process. If Quiet Boot is enabled, the Hit 'DEL" message will not display.
  - If [Enabled] is selected, the BIOS will place the "Press 'DEL' to enter Setup" message on screen during the boot process, to indicate when you may press 'DEL' to enter the BIOS Setup Utility menus.

- Interrupt 19 Capture – [***Disabled***] or [Enabled]
  - If [Disabled] is selected, allows the BIOS to prevent option ROMs from trapping interrupt 19.
  - If [Enabled] is selected, allows option ROMs to trap interrupt 19.

- Watchdog Timeout in Seconds – [***Disabled***] or [1-255]
  - If this field [1-255] is enabled by selecting a time interval (select a whole number between 1 and 255 seconds), it will direct the watchdog timer to reset the system if it fails to boot the OS properly. Refer to the watchdog timer section in Chapter 3 for more information.

>**Boot Device Priority**

Use these fields to determine the sequence (boot order) the BIOS checks for a boot device. You change the boot order by selecting from the list of the available boot devices, as well as, changing the order of the device types. Refer to the following examples, including the device types.

- 1st Boot Device – [1st Floppy Drive], [HDD: Mfg + model], [CD/DVD], [Network: IBA xE Slo], or [Disabled]
  - Example [**1st Floppy Drive**]
- 2nd Boot Device – [1st Floppy Drive], [HDD: Mfg + model], [CD/DVD], [Network: IBA xE Slo], or [Disabled]
  - Example [**CD/DVD: Mfg, model**]
- 3rd Boot Device – [1st Floppy Drive], [HDD: Mfg + model], [CD/DVD], [Network: IBA xE Slo], or [Disabled]

- Example [**HDD: Mfg, model**]

- 4th Boot Device – [1st Floppy Drive], [HDD: Mfg + model], [CD/DVD], [Network:IBA xE Slo], or [Disabled]
  - Example [**Network:IBA xE Slo**] (onboard Ethernet 2 connection)

Changing Boot Order (Swap) Example:

1. Scroll to the 1st Boot Device [1st Floppy Drive] and press the <**Enter**> key.

   The Options list appears with all of the detected devices listed including [Disabled] as an option. Only the 1st Drive selections from the device types (Hard Disk, Removable, and CD/DVD) will be shown in the popup menu. See Figure 4-5.

   If you want to change from a standard floppy drive to a USB floppy drive, go to the Removable Drives list, where you can select the device that appears in the list instead of the 1st Floppy Drive.

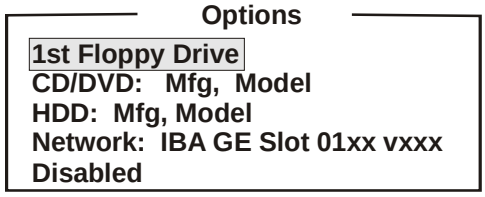


Figure 4-5. Boot Options Popup Menu Example

2. Scroll down the popup menu list and select another device, such as the CD-ROM in the 2nd Boot Device position and press the <**Enter**> key.

   The CD-ROM changes or swaps place with the 1st Floppy Drive, while at the same time putting the 1st Floppy Drive in the 2nd Boot Device position (former location of the CD-ROM).

3. If you select [Disabled], the 1st Floppy Drive moves to the 4th position (last), and changes to *Disabled*, while all other devices move up in the Boot order.

The following device type fields are dependent on the type and number of devices connected to the system. For example, you may not see the CD/DVD type field if there are no CD-ROMs or DVDs connected to the system, including USB CD/DVDs.

>**Hard Disk Drives**

This option specifies the boot sequence from the available Hard Disk Drives (HDD). This option and the number of HDDs only appears on screen if the BIOS detects Hard Disk Drives (HDD) attached to the system, including USB HDDs.

- 1st Drive – [HDD: Mfg + Model], [HDD: Mfg + Model], or [Disabled]

  The 1st Drive in this list is the only device to appear in the Boot Device Priority list. The remaining fields are dependent on the number of HDD devices detected by the BIOS, including the compact flash card. Use the swap example described earlier when changing the order of these devices.

- 2nd Drive – [HDD: Mfg + Model], [HDD: Mfg + Model], [HDD: Mfg + Model], or [Disabled]
- 3rd Drive – [HDD: Mfg + Model], [HDD: Mfg + Model], [HDD: Mfg + Model], or [Disabled]

>**Removable Drives**

This option specifies the boot sequence from the available Removable Drives. The number and type of devices only appear on screen if the BIOS detects more than one Removable Drive attached to the system, including USB floppy drives, Zip drives, etc.

- 1st Drive – [1st Floppy Drive], [USB: Mfg + model or device type], [USB: Mfg + model or device type], or [Disabled]

The 1st Drive in this list is the only device to appear in the Boot Device Priority list. The remaining fields and options are dependent on the number of removable devices detected by the BIOS. Use the swap example described earlier when changing the order of these devices.

- 2nd Drive – [1st Floppy Drive], [USB: Mfg + model or device type], [USB: Mfg + model or device type], [USB: Mfg + model or device type], or [Disabled]
- 3rd Drive – [1st Floppy Drive], [USB: Mfg + model or device type], [USB: Mfg + model or device type], [USB: Mfg + model or device type], or [Disabled]
- 4th Drive – [1st Floppy Drive], [USB: Mfg + model or device type], [USB: Mfg + model or device type], [USB: Mfg + model or device type], or [Disabled]

>**CD/DVD Drives**

This option specifies the boot sequence from the available CD/DVDs. This option only appears on screen if the BIOS detects any CD/DVDs, including USB CD/DVDs, attached to the system. Use the swap example described earlier when changing the order of these devices.

- 1st Drive – [CD/DVD: Mfg + Model] or [Disabled]

  The 1st Drive in this list is the only device to appear in the Boot Device Priority list. The remaining fields and options are dependent on the number of CD/DVD devices detected by the BIOS.

- 2nd Drive – [CD/DVD: Mfg + Model], [CD/DVD: Mfg + Model], or [Disabled]

Security Menu Screen

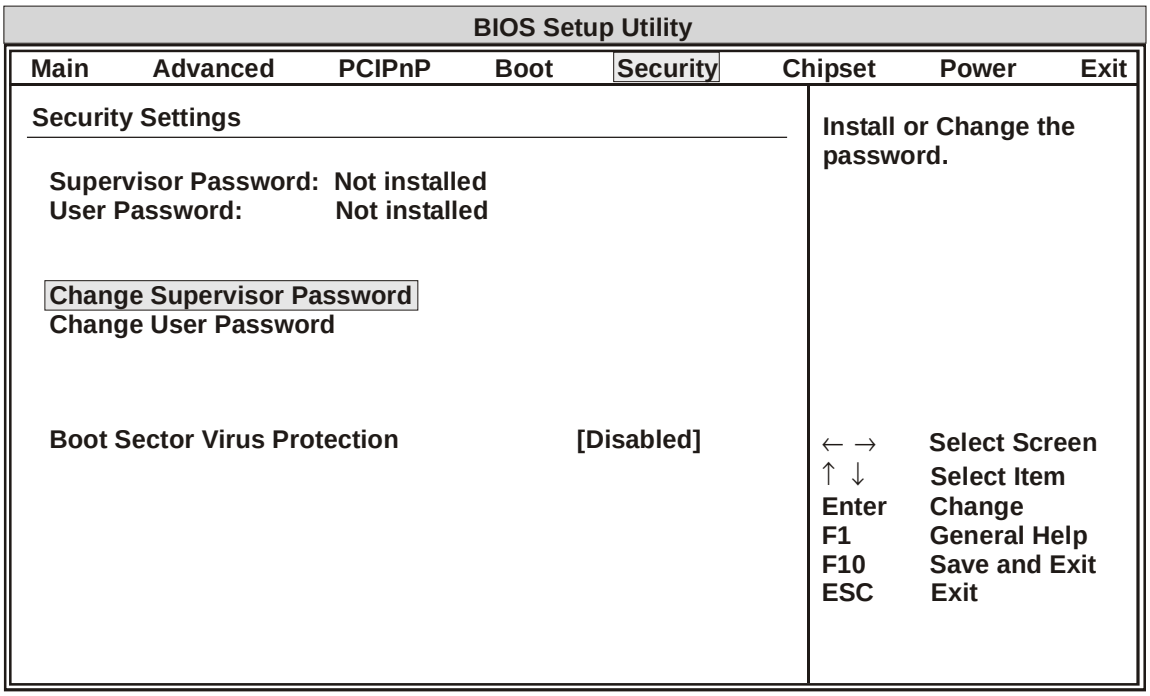


Figure 4-6. Security Menu Screen

Security Settings

- Supervisor Password – [***Not Installed***] or (Set - no indication)

  Indicates if a supervisor password has been set.

  * If the password has been installed, Installed appears on screen.
  * If no the password has be selected, then Not Installed appears on screen.

- User Password – [***Not Installed***] or (Set - no indication)

  Indicates if a user password has been set. If the password has been installed, Installed displays. If not, Not Installed displays.

- Change Supervisor Password

  a. Select **Change Supervisor Password** from the Security Setup menu.

  b. Press <*Enter*> to access the pop-up menu, *Enter New Password:*

  c. Type the password and press <*Enter*> again.

  The screen will not display the password as you type.

  d. Retype the password when prompted by the pop-up menu and press <*Enter*> again.

  * If the password is confirmed, [Installed] will appear on screen in place of [Not Installed] and the password will be stored in NVRAM.
  * If the password is not confirmed when you retype it, an error message will appear. Follow the on screen instructions to correct the situation, or clear the password and start over.

If the Supervisor Password field is "Installed", the following item appears on the screen.

- User Access Level – [No Access] or [View Only], [LIMITED], or [***Full Access***]

To clear Supervisor password: .

a. Press <*Enter*> to access the pop-up menu, *Enter New Password:*

b. Do not enter a password and press the <*Enter*> key, following the prompts.

c. Repeat this process until the old password is gone, which is indicated by *Not Installed*.

- Change User Password

a. Select **Change User Password** from the Security Setup menu.

b. Press <*Enter*> to access the pop-up menu, *Enter New Password:*

c. Type the password and press <*Enter*> again.

The screen will not display the password as you type.

d. Retype the password when prompted by the pop-up menu and press <*Enter*> again.

* If the password is not confirmed when you retype it, an error message will appear.
* If the Change User Password field is "Installed", a Pop-Up screen, titled "Clear User Password?" appears with these selections.

- Clear User Password – [***OK***] or [Cancel]
- Password Check – [***Setup***] or [Always]

- Boot Sector Virus Protection – [***Disabled***] or [Enabled]

This field displays a warning when any program (or virus) issues a Disk Format command or attempts to write to the boot sector of the hard disk drive.

* If [Disabled] is selected, there is no Boot Sector Virus Protection warning displayed for the hard disk drive.
* If [Enabled] is selected, a warning is displayed when any program (or virus) issues a Disk Format command or attempts to write to the boot sector of the hard disk drive. A warning display also appears if there is any attempt to format any cylinder, head, or sector of any hard disk drive.

The following display appears when a write is attempted to the boot sector.

```
Boot Sector Write!
Possible VIRUS: Continue (Y/N)?
```

You may have to type N several times to prevent the boot sector write.

The following appears after any attempt to format any cylinder, head, or sector of any hard disk drive via the BIOS INT 13 Hard disk drive.

```
Service:
Format!!!
Possible VIRUS: Continue (Y/N)?
```

Chipset Setup Screen

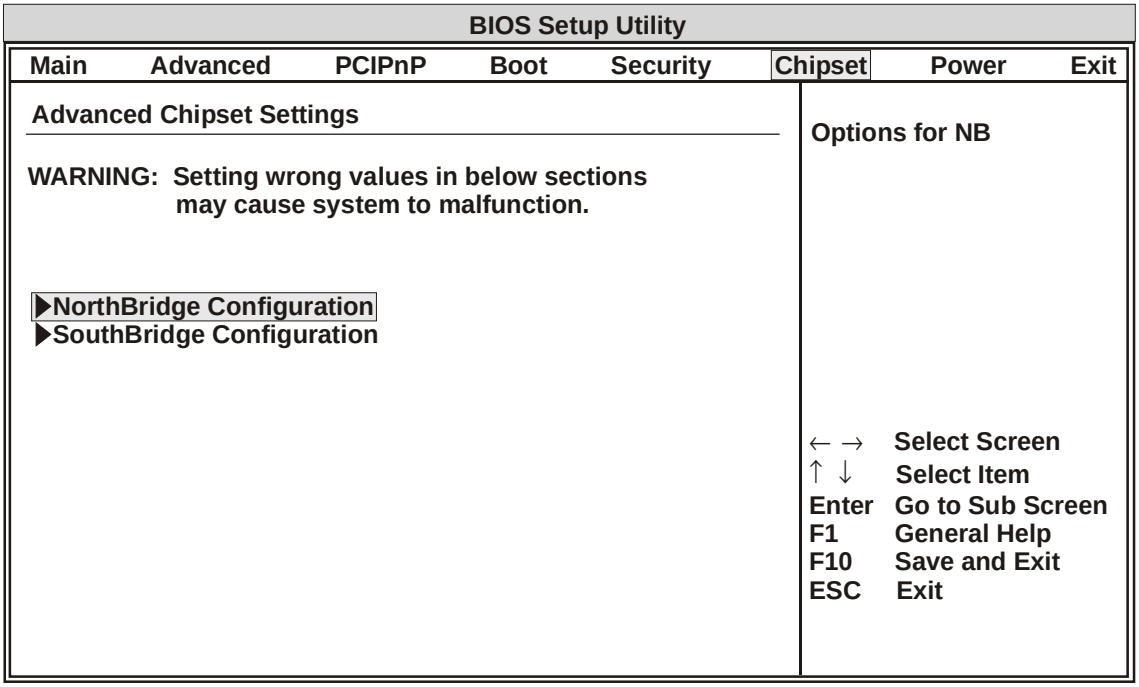


Figure 4-7. Chipset Setup Screen

Advanced Chipset Settings

>**NorthBridge Chipset Configuration**

- DRAM Frequency – [*200 MHz*], [266 *MHz*], [333 *MHz*], or [**Auto**]
- Configure DRAM Timing by SPD – [Disabled] or [***Enabled***]
  - ∗ If [Disabled] is selected, the following items appear on screen.
  - ♦ DRAM CAS# Latency – [***2.5***] or [2]
  - ♦ DRAM RAS# Precharge – [2 Clocks] or [***3 Clocks***]
  - ♦ DRAM RAS# to CAS# Delay – [2 Clocks] or [***3 Clocks***]
  - ♦ DRAM Precharge Delay – [5 Clocks], [6 Clocks], or [***7 Clocks***]
  - ♦ DRAM Burst Length – [*4*] or [**8**]
- Memory Hole – [***Disabled***] or [15MB-16MB]
- Init. Graphics Adapter Priority – [Internal VGA] or [***PCI/Int-VGA***]
- Internal Graphics Mode Select – [Disabled], [Enabled, 1 MB], [Enabled, 4 MB], [***Enabled, 8 MB***], [Enabled, 16 MB], or [Enabled, 32 MB]
- Graphics Aperture Size – [***64 MB***], [128 MB], or [256 MB]

  Video Function Configuration

  - ♦ DVMT Mode Select – [Fixed Mode], [DVMT Mode], or [***Combo Mode***]
  - ♦ Boot Display Device – [***Auto***], [CRT], [LFP], or [CRT + LFP]

- Flat Panel Type [***None***]

  Refer to Table 4-3 for the list of supported resolutions and flat panel types. Some flat panels may require video BIOS modifications. It you think this is the case, or would like help in setting up your flat panel, contact Ampro for assistance with the flat panel adaptation.

- Local Flat Panel Scaling – [***Auto***], [Forced Scaling], or [Disabled]

Table 4-3. Flat Panel Type List

#	LCD Resolution	BITs
0	***None***	
1	640 x 480 LVDS	
2	800 x 600 LVDS	
3	1024 x 768 LVDS	24 bits
4	1280 x 1024 LVDS	
5	1400 x 1050 LVDS	
6	1024 x 768 LVDS	18 bits
7	1600 x 1200	48 bits
8	1280 x 1024	48 bits

#	LCD Resolution	BITs
9	800 x 600	24 bits
10	800 x 600	18 bits
11	1024 x 768	36 bits

>**SouthBridge Configuration**

- Onboard AC'97 Audio – [***Auto***] or [Disabled]
- Restore on AC Power Loss – [Power Off], [***Power On***], or [Last State]
  - If [Power Off] is selected, the power is held off until the power button is pressed.
  - If [Power On] is selected, the power is restored to the computer, as soon as, AC power is available.
  - If [Last State] is selected, power is restored to the previous power state before the power loss actually occurred.

NOTE

This feature only operates with an ATX type power supply. The term *AC power loss* used in this context refers to the loss of the standby voltage on the 5V_SB pins and is continuously monitored after the system is turned off. If the standby voltage is not detected after 30 seconds, then it is considered an AC power loss condition. If the standby voltage remains stable for 30 seconds, then it is assumed that the system was switched off properly.

If you use an inexpensive ATX power supply, you may experience a short AC power sag, where the system turns off but does not switch back on. This can occur even when the PS_ON# signal is asserted correctly by the module. In this case, the internal circuitry of the ATX power supply has become confused. Usually another AC power off/on cycle is necessary to recover from this situation.

The ReadyBoard 800 does not require a CMOS battery to support the *Power Loss Control* feature.

Power Menu Screen

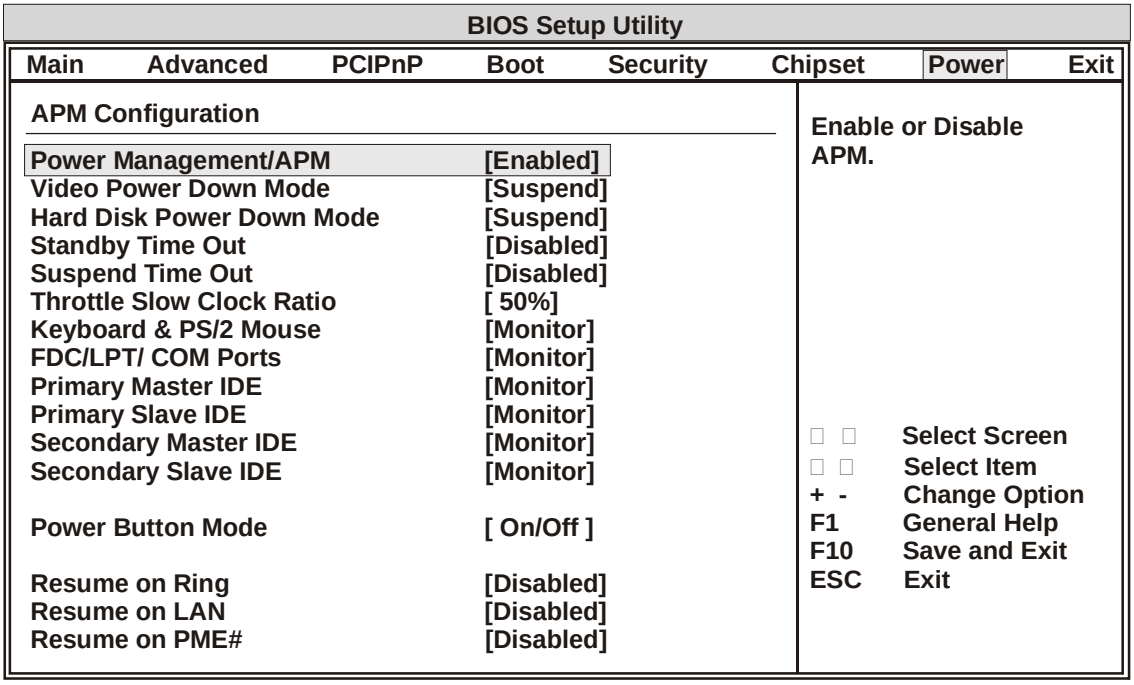


Figure 4-8. Power Menu Screen

APM Configuration

This power management feature is an older standard and may not be as widely supported today as it once was. The current preference for power management control is ACPI. The settings in this menu apply equally to the APM or ACPI power management.

- Power Management/APM – [Disabled] or [***Enabled***]

  This field enables power management for APM or ACPI. The ACPI feature is [Enabled] in the default settings under the Advanced menu.

  - If [Enabled] is selected, the following items appear on the screen.
  - Video Power Down Mode – [*Disabled*], [Standby] or [**Suspend**]
    - If [Disabled] is selected, the BIOS is prevented from initiating any power saving modes related to the video display or the monitor.
    - If [Standby] is selected, the monitor is placed into standby mode after the specified period of display inactivity has expired. The monitor screen appears blacked out, but the monitor remains powered in a low state.
    - If [Suspend] is selected, the monitor is placed into a suspended mode after the specified period of display inactivity has expired. The monitor screen appears blacked out, but the monitor remains powered in a low state.

- Hard Disk Drive Power Down Mode – [*Disabled*], [Standby] or [**Suspend**]
  - If [Disabled] is selected, the hard disk drive (HDD) is prevented from going into a power down mode.
  - If [Standby] is selected, the hard disk drive (HDD) is stopped from spinning during this standby mode.
  - If [Suspend] is selected, the power to the hard disk drive (HDD) is removed during this system suspend state.
- Standby Time Out – [***Disabled***], [1 Min], [2 Min], [4 Min], [8 Min], [10 Min], [20 Min], [30 Min], [40 Min], [50 Min], or [60 Min]
  - If [Disabled] is selected, the system is prevented from entering the standby mode.
  - If [1 to 40] is selected, the system enters standby mode after being inactive for the specified number of minutes, such as, 1 minute, 2 minutes, 4 minutes, etc.
- Suspend Time Out – [***Disabled***], [1 Min], [2 Min], [4 Min], [8 Min], [10 Min], [20 Min], [30 Min], [40 Min], [50 Min], or [60 Min]
  - If [Disabled] is selected, the system is prevented from entering the suspend mode.
  - If [1 to 60] is selected, the system enters suspend mode after being inactive for the specified number of minutes, such as, 1 minute, 2 minutes, 4 minutes, etc.
- Throttle Slow Clock Ratio – [87.5%], [75.0%], [62.5%], [***50%***], [37.5%], [25%], or [12.5%]

  This field allows the BIOS to throttle the CPU clock to reduce power consumption by the percentage selected.

  Selecting [87.5% to 12.5%] allows the BIOS to throttle back the CPU clock and operate a the percentage specified. For example, a throttle ratio of 50% means the clock is turned off during half of it its normal operational time. Selecting 87.5%, means the CPU clock is operating 87.5% of the time.
- Keyboard & PS/2 Mouse – [Ignore] or [***Monitor***]
  - If [Monitor] is selected, the activity of the Keyboard & PS/2 Mouse can wake up the system from a power management state.
  - If [Ignore] is selected, the Keyboard & PS/2 Mouse will not wake up the system from a power management state.
- FDC/LPT/COM Ports – [Ignore] or [***Monitor***]
  - If [Monitor] is selected, the activity on the FDC/LPT/COM Ports can wake up the system from a power management state.
  - If [Ignore] is selected, the FDC/LPT/COM Ports will not wake up the system from a power management state.
- Primary master IDE – [Ignore] or [***Monitor***]
  - If [Monitor] is selected, activity on the Primary Master IDE channel can wake up the system from a power management state.
  - If [Ignore] is selected, activity on the Primary Master IDE channel will not wake up the system from a power management state.
- Primary slave IDE – [Ignore] or [***Monitor***]
  - If [Monitor] is selected, activity on the Primary Slave IDE channel can wake up the system from a power management state.
  - If [Ignore] is selected, activity on the Primary Slave IDE channel will not wake up the system from a power management state.

- Secondary master IDE – [Ignore] or [***Monitor***]
  - If [Monitor] is selected, activity on the Secondary Master IDE channel can wake up the system from a power management state.
  - If [Ignore] is selected, activity on the Secondary Master IDE channel will not wake up the system from a power management state.
- Secondary slave IDE – [Ignore] or [***Monitor***]
  - If [Monitor] is selected, activity on the Secondary Slave IDE channel can wake up the system from a power management state.
  - If [Ignore] is selected, activity on the Secondary Slave IDE channel will not wake up the system from a power management state.

- Power Button Mode – [***On/Off***] or [Suspend]

  This field allows you to activate the Power Button for use with sleep states and it will transition the system between power on and sleep states. This feature is also OS dependent as well.

- Resume On Ring – [***Disabled***] or [Enabled]
- Resume On LAN – [***Disabled***] or [Enabled]
- Resume On PME# – [***Disabled***] or [Enabled]
  - Resume on RTC Alarm – [***Disabled***] or [Enabled]

    If Resume on RTC Alarm is [Enabled] the following fields appear on screen.
    - RTC Alarm Date (Days) – [Every Day], [01], [02], [03], [04], [05], [06], [07], [08], [09], [10], [11], [12], [13], [14], [***15***], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], or [31]
    - System Time – [***12:30:30***]

Exit and Default Menu Screen

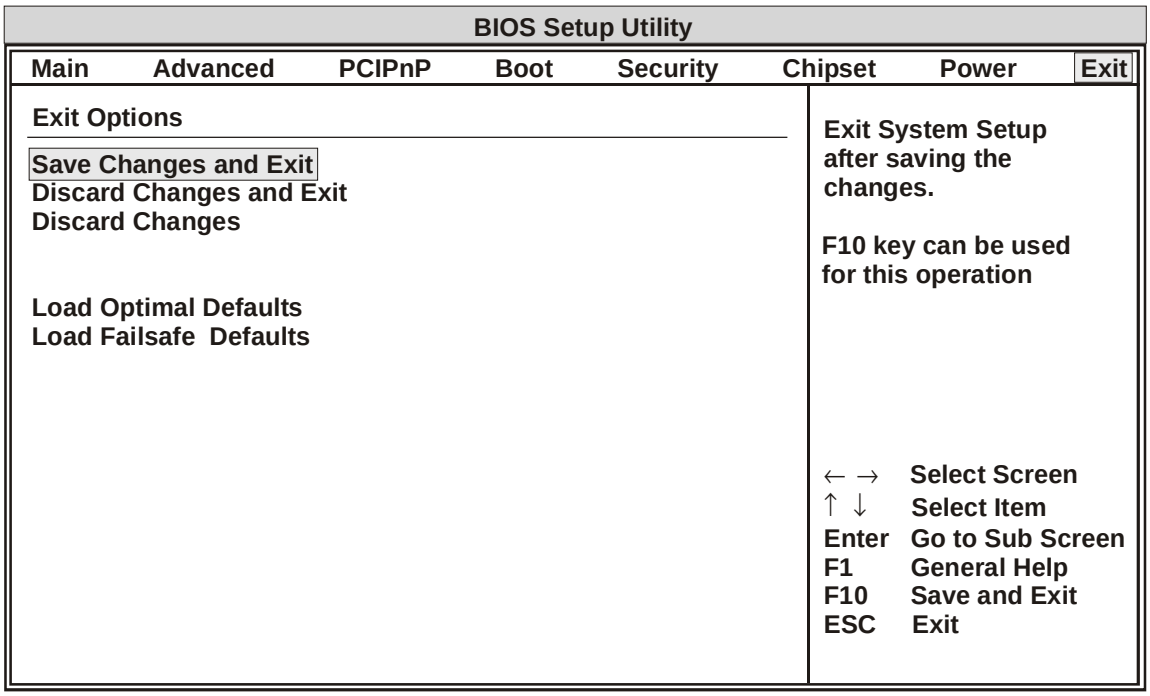


Figure 4-9. Exit and Default Menu Screen

Exit Options

- Save Changes and Exit

  This selection allows you to leave Setup, saving your changes, and rebooting the system so the new BIOS Setup Utility configuration parameters can take effect.

  - Select **Save Changes and Exit** from the Exit Options menu and press <*Enter*>.

    The following text appears on screen:

    ```
    Save Configuration Changes and Exit Now?

    [Ok] [Cancel]
    ```

  - Select *Ok* to save changes and exit.

  The < F10 > key can also be used for this operation.

- Discard Changes and Exit

  This selection allows you to quit Setup without making any permanent changes to the BIOS Setup Utility system configuration.

  - Select **Discard Changes and Exit** from the Exit Options menu and press <*Enter*>.

    The following text appears on screen:

    ```
    Discard Changes and Exit Setup Now?

    [Ok] [Cancel]
    ```

- Select *Ok* to discard changes and exit.

The < ESC > key can also be used for this operation.

- Discard Changes

  This selection allows you to discard any changes made to BIOS Setup Utility without leaving BIOS Setup Utility.

  - Select **Discard Changes** from the Exit menu and press <*Enter*>.

    The following text appears on screen:

```
Discard Changes?

[Ok] [Cancel]
```

  - Select *Ok* to discard changes.

The < F7 > key can also be used for this operation.

Loading Defaults

- Load Optimal Defaults

  This selection automatically sets all BIOS Setup Utility options to a complete set of default Optimal settings. The Optimal settings are designed for maximum system performance, but may not work best for all system applications. In particular, do not use the Optimal setup options if your system is experiencing system configuration problems.

  - Select **Load Optimal Defaults** from the Exit menu and press <*Enter*>.

    The following text appears on screen:

```
Load Optimal Defaults?

[Ok] [Cancel]
```

  - Select *Ok* to load Optimal defaults.

The < F9 > key can also be used for this operation.

- Load Failsafe Defaults

  This selection automatically sets all BIOS Setup Utility options to a complete set of default Fail-Safe settings. The Fail-Safe settings are designed for maximum system stability, but not maximum performance. Select the Fail-Safe Setup options if your system is experiencing system configuration problems.

  - Select **Load Fail-Safe Defaults** from the Exit menu and press <*Enter*>.

    The following text appears on screen:

```
Load Fail-Safe Defaults?

[Ok] [Cancel]
```

  - Select *Ok* to load Fail-Safe defaults.

The < F8 > key can also be used for this operation.

Appendix A Technical Support

Ampro Computers, Inc. provides a number of methods for contacting Technical Support listed in the Table A-1 below. Requests for support through the Virtual Technician are given the highest priority, and usually will be addressed within one working day.

- Ampro Virtual Technician – This is a comprehensive support center designed to meet all your technical needs. This service is free and available 24 hours a day through the Ampro web site at http://ampro.custhelp.com. This includes a searchable database of Frequently Asked Questions, which will help you with the common information requested by most customers. This is a good source of information to look at first for your technical solutions. However, you must register online if you wish to use the "Ask a Question" feature.
- Personal Assistance – You may also request personal assistance by going to the "Ask a Question" area in the Virtual Technician. Requests can be submitted 24 hours a day, 7 days a week. You will receive immediate confirmation that your request has been entered. Once you have submitted your request, you must log in to go to the "My Stuff" area where you can check status, update your request, and access other features.
- Embedded Design Resource Center – This service is also free and available 24 hours a day at the Ampro web site at http://www.ampro.com. However, you must be registered online before you can login to access this service.

  The Embedded Design Resource Center was created as a resource for embedded system developers to share Ampro's knowledge, insight, and expertise gained from years of experience. This page contains links to White Papers, Specifications, and additional technical information.

Table A-1. Technical Support Contact Information

Method	Contact Information
Virtual Technician	http://ampro.custhelp.com
Web Site	http://www.ampro.com
Standard Mail	Ampro Computers, Incorporated 5215 Hellyer Avenue San Jose, CA 95138-1007, USA

Appendix B LAN Boot Feature

This Appendix describes the LAN Boot feature provided by the ReadyBoard 800. The balance of this appendix briefly describes how to set up LAN Boot using the PXE boot agent BIOS settings. The LAN Boot feature is not enabled or disabled in the ReadyBoard 800 BIOS Setup Utility, but its boot order can be changed.

Introduction

LAN Boot is supported by a single Ethernet port on the ReadyBoard 800, and is based on the Preboot Execution Environment (PXE), an open industry standard. PXE (pronounced *pixie*) was designed by Intel, along with other hardware and software vendors, as part of the Wired for Management (WfM) specification to improve management of desktop systems. This technology can also be applied to the embedded system market place. PXE turns the ReadyBoard 800 Ethernet ports into boot device when connected over a network (LAN).

PXE boots the ReadyBoard 800 from the network (LAN) by transferring a *boot image file* from a server. This image file is typically the operating system for the ReadyBoard 800, or a pre-OS agent that can perform management tasks prior to loading the image file (OS). A management task could include scanning the hard drive for viruses before loading the image file.

PXE is not operating system-specific, so the image file can load any OS. The most common application of PXE (LAN Boot) is installing an OS on a brand new device (hard disk drive) that has no operating system, (or reinstalling it when the operating system has failed or critical files have been corrupted).

Using PXE prevents the user from having to manually install all of the required software on the storage media device, (typically a hard disk drive) including the OS, which might include a stack of installation CD-ROMs. Installing from the network is as simple as connecting the ReadyBoard 800 to the network and powering it on. The server can be set up to detect new devices and install software automatically, thereby greatly simplifying the management of small to large numbers of systems attached to a network.

If the hard disk drive should crash, the network can be set up to do a hardware diagnostic check, and once a software-related problem is detected, the server can re-install the defective software, or all the ReadyBoard 800 software from the server. Booting from the network also helps ensure a *clean* boot, with no boot-time viruses or user-modified files. The boot files are stored on the PXE server, protected from infection and user-modification.

To effectively make use of the Ampro supplied feature (LAN Boot), a PXE boot agent (included with ReadyBoard 800 BIOS) and a PXE server are required. The PXE server is designed to work in conjunction with a Dynamic Host Configuration Protocol (DHCP) server and also requires a TFTP (Trivial File Transfer Protocol) server installed on the same system. The PXE server can be shared with a DHCP server or installed on a different server and may require additional PXE server components. This makes it possible to add PXE to an existing network without affecting the existing DHCP server or its configuration. Refer to the LAN Boot directory on the ReadyBoard 800 Doc & SW CD-ROM and the web sites listed here for more information on PXE boot agents, PXE servers, and PXE components. For a more detailed technical description of how PXE works, go to, http://www.pxe.ca. For more detailed information concerning pre-OS agents, go to: http://www.pre-OS.com.

Ampro has provided an Intel® PXE boot agent integrated into the ReadyBoard 800 BIOS, but does not provide the PXE server or its components. You will need to provide your own PXE server and its components, before making full use of the LAN Boot feature. When you change the BIOS settings to move LAN Boot to the top of the boot order, you will need to exit the BIOS Setup Utility, saving your changes, and reboot the system to enter and set the PXE Boot Agent BIOS settings. Refer to *Accessing PXE Boot Agent BIOS Setup Utility* on the next page for more setup and configuration information.

Accessing PXE Boot Agent BIOS Setup Utility

The Intel PXE Boot agent is integrated into the ReadyBoard 800 BIOS and only supports one protocol, the Wired for Management (WfM) 2.0 specification for Preboot eXecution Environment (PXE). There are no options or fields in the ReadyBoard 800 BIOS Setup Utility to disable or enable the LAN Boot feature.

The LAN Boot feature can be moved to the top of the boot order, and will be detected if an Ethernet connection is available. The BIOS autodetects the Ethernet connection and searches for the PXE server and boot image as soon as you boot the system.

To access PXE Boot Agent BIOS Setup Utility when you want to use the LAN Boot feature, refer to this procedure:

1. Connect a Ethernet cable to the ReadyBoard 800 and reboot the system.
2. Access the PXE Boot Agent BIOS Setup Utility by pressing the Ctrl + S keys, when the following message appears on the boot screen.

```
Initializing Intel (R) Boot Agent GE vx.x.xx
PXE v2.0 Build 0xx (WfM 2.0)
Press Ctrl + S to enter the setup Menu…
```

3. If you miss this message, reboot the system and press Ctrl + S early in the boot process.
4. Select from the menu options when the PXE Boot Agent screen appears similar to the one shown in Figure B-1.
5. Follow the instructions at the bottom of the screen to navigate through the selections and modify any settings.
6. Save your changes (F4) and reboot the system.

   When you reboot the system the PXE Boot Agent will make up to two attempts to find and load the boot image using a DHCP server (PXE Server). Messages similar to the ones listed here may appear, however briefly, on screen.

```
Intel (R) Boot Agent GE v1.x.xx
Copyright © 1997-2005, Intel Corporation


Intel (R) Boot Agent PXE base Code (PXE-2.1 build 084)
Copyright © 1997-2005, Intel Corporation


Initializing and Establishing Link…… (BIOS detecting Ethernet link)


Client Mac Addr:  xx xx xx xx xx xx GUID: xxxxxxxx xxxx xxxxx……
DHCP ……/  (looking for PXE server and boot filename)



(If errors occur, you might see some of the following messages)
PXE-E53:  No boot filename received (no boot filename found)


Or
```

PXE-E61: Media test failure, check cable (no cable connection)

PXE-M0F: Exiting Intel Boot Agent

PXE Boot Agent Setup Screen

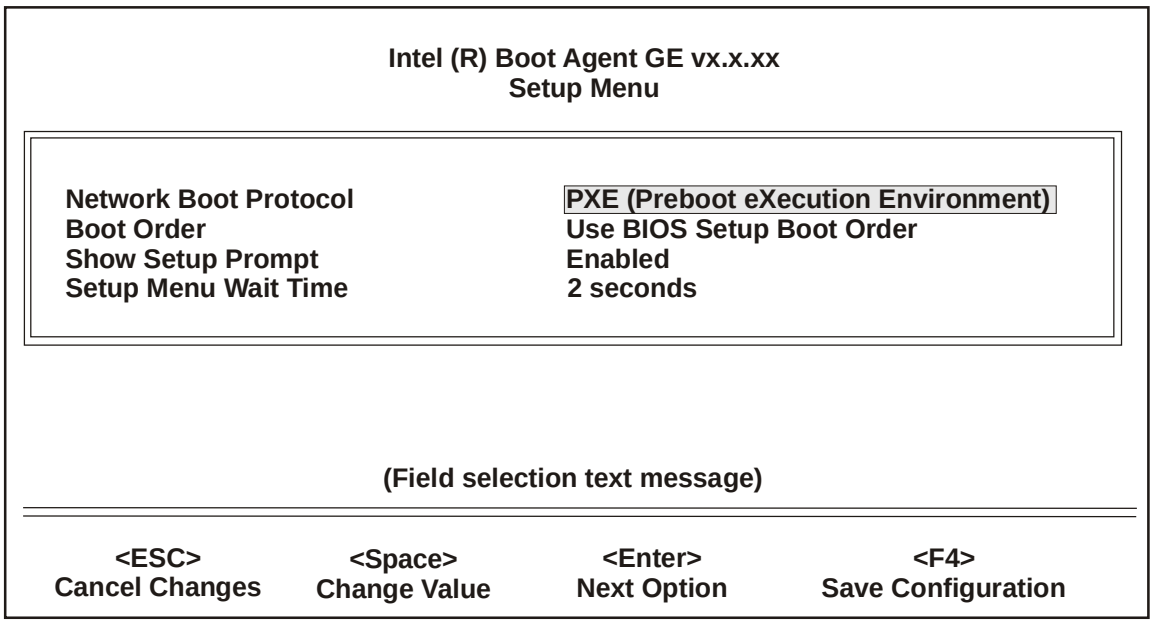


Figure B-1. PXE Agent Boot Setup Screen

- **PXE Boot Agent Setup**
  - Network Boot Protocol – [**PXE (Preboot eXecution Environment)]**

    This is the only option for this field.
  - Boot Order – [**Use BIOS Setup Utility Boot Order**]

    This is the only option for this field. Selects order in which boot devices are queried.
  - Show Setup Prompt – [Disabled] or [**Enabled**]

    If [**Enabled**] is selected, Ctrl + S message will appear during initialization.
  - Setup Menu Wait Time – [0 seconds], [**2 seconds**], [3 seconds], or [5 seconds]

NOTE	The default values are shown highlighted (**bold text**) in the list of options on the this page. Refer to the bottom of the Setup screen for navigation instructions when making selections.

Alternate Method of Selecting LAN Boot

The boot process reveals an alternate method of accessing the Network (LAN Boot) if your monitor powers up quickly enough. You will see a text line similar to the one shown below immediately after the *Press <Del> to enter Setup* message displayed on screen.

```
Press F12 if you want to boot from the Network
```

You can use this feature to skip going to BIOS Setup to move [Network:…] ahead of the other boot devices and set the Network (PXE Boot Agent) to boot the system.

1. Press **F12** to boot the system using the LAN Boot (PXE) feature.

   This selects the network (Onboard LAN or Network: IDA …) ahead of the other boot devices for the current boot and you will see the text line change to the following message.

```
Network selected as first boot device for the current boot
```

   Once this text message appears on screen, you should see the system going through the cycle of booting from the Network shown in the earlier examples in this Appendix.

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